Bidirectional Asynchronous Generator and Battery Interface Circuit

by

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Thesis presented in partial fulfilment of the requirements for the degree of Master of Engineering (Electrical) in the Faculty of Engineering at Stellenbosch University

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Declaration

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Abstract

In some instances additional power is required to support an electrical load on board an aircraft. A ram air turbine (RAT) generator can be used to supply the necessary power in conjunction with a storage unit such as a battery or supercapacitors. The RAT is driven by the airflow surrounding the sub-sonic aircraft and acts as the main power supply. The storage unit is charged when the RAT is supplying excess power or when the load is disconnected.

This thesis presents the design and implementation of a prototype circuit that demonstrates the interface between a generator and a battery of electrochemical cells to an electrical load. To simulate the airflow through the turbine an asynchronous machine is employed to turn the shaft of an asynchronous generator. The prototype circuit is designed such that the battery is connected to a dc bus through a bidirectional dc-dc converter and the asynchronous machine interfaces with the dc bus through a bidirectional inverter. The load is connected between the positive and negative dc bus rails.

The dc-dc converter circuit functions to regulate the dc bus voltage by utilising a double control loop strategy with an inner and outer control loop. The inverter functions as a synchronous rectifier and the power delivered to the dc bus from the generator is controlled as a function of the converter's battery voltage. The simulated and measured test results of the complete system are compared and presented.

Opsomming

In sommige gevalle benodig vliegtuie addisionele krag om 'n elektriese las van krag te voorsien. 'n Klein lugaangedrewe turbine kan gebruik word om die addisionele krag te voorsien in samewerking met 'n stooreenheid soos 'n battery of superkapasitor. Die stooreenheid word herlaai wanneer die lugaangedrewe turbine oortollige krag lewer aan die stelsel of wanneer die las ontkoppel word.

Hierdie tesis bespreek die ontwerp en implementering van 'n prototipe stroombaan wat die werking tussen 'n generator en battery demonstreer. 'n Asinkroon motor word gebruik om die lugvloei deur die turbine te simuleer en die dryfas van die asinkroon generator aan te dryf. Die battery word gekoppel aan 'n gs bus deur middel van 'n bidireksionele gs-gs omsetter en die generator word gekoppel aan die gs bus deur middel van 'n bidireksionele ws-gs omsetter. Die las word gekoppel tussen die positiewe en negatiewe gs bus lyne.

Die gs-gs omsetter funksioneer om die gs busspanning te reguleer deur middel van 'n dubbelle beheerlus strategie wat bestaan uit 'n binneste en buitenste beheerlus. Die ws-gs omsetter funksioneer as 'n sinkroon gelykrigter waar die krag wat aan die gs bus gelewer word, beheer word as 'n funskie van die gs-gs omsetter se battery spanning. Die gesimuleerde en gemete resultate vir die volledige stelsel word vergelyk en voorgelê.

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Nomenclature

Variables

f_s	switching frequency	[kHz]
i_{dc}	instantaneous dc bus current	[A]
i_L	instantaneous inductor current	[A]
m_a	modulation index	[ ]

Abbreviations

ac	alternating current
ADC	analog-to-digital converter
DAC	digital-to-analog converter
dc	direct current
DSP	digital signal processor
emf	electromotive force
IC	integrated circuit
IGBT	insulated-gate bipolar transistor
LUT	lookup table
mmf	magnetomotive force
MOSFET	metal-oxide-semiconductor field-effect transistor
MPPT	maximum power point tracking
NTC	negative temperature coefficient
PCB	printed circuit board
PI	proportional-integral
PWM	pulse-width modulation
RAT	ram air turbine
rms	root mean square
VSD	variable-speed drive
VSI	voltage source inverter

Chapter 1

Introduction

1.1 Background

In order to support an electrical load on board an aircraft, additional power is required. For this application a ram air turbine (RAT) generator can be used to supply the necessary power in conjunction with a storage unit such as a battery or supercapacitors. The RAT is driven by the airflow surrounding the sub-sonic aircraft and acts as the main power supply providing average power to a load. Generally the storage unit is only used to supply power during transient conditions [1]. If however the RAT is unable to supply the required power due to a lack of airflow, the storage unit supplies the necessary power until it is depleted. The storage unit is charged when the RAT is supplying excess power.

A prototype circuit that demonstrates the interface between an air-powered turbine generator and a battery of electrochemical cells to an electrical load on board an aircraft is proposed. To simulate the airflow through the turbine an asynchronous machine is employed to turn the shaft of an asynchronous generator. A speed-varying inverter will be used to control the voltage and frequency applied to the stator windings of the driving machine, thus simulating varying airflow conditions. A deep-cycle lead-acid battery will be used as the storage unit. The layout of the proposed circuit is shown in Fig. 1.1.

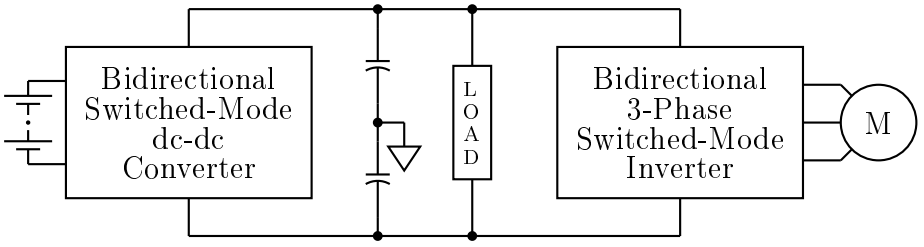

Figure 1.1: Block digram of a bidirectional battery and machine interface circuit.

The battery is connected to a dc bus through a non-isolated bidirectional dc-dc converter and the asynchronous machine interfaces with the dc bus through a non-isolated bidirectional inverter. The interface is required to transfer up to 2 kW of electrical power between the battery and asynchronous machine. The load is connected between the positive and negative dc bus rails. The proposed nominal dc bus voltage is 350 V rail-to-rail. A reasonably high bus voltage is used to reduce the current within the dc bus, thus reducing self-heating while improving the efficiency of the power distributed to the load.

The dc-dc converter is bidirectional to facilitate extended periods of regenerative braking (during which energy is returned to the battery). The converter is required to be current-controlled and voltage-regulated. As such the direction of current to or from the batteries will be regulated as a function of the dc bus voltage.

The inverter circuit will function as a synchronous rectifier to facilitate the flow of current from the asynchronous machine to the dc bus whilst airborne.

1.2 Thesis Objectives

The thesis objectives can be divided into three parts. The first objective is to design, manufacture and test the bidirectional non-isolated current-controlled voltage-regulated switched-mode dc-dc converter that is required to interface a bank of batteries to a dc bus. The bidirectional transfer of up to 2 kW electrical power between a nominally 350 V dc bus and a bank of batteries is to be demonstrated. The efficiency of the converter is to be determined. A closed-loop control circuit is required for the design of the converter and will be analysed before manufacturing the prototype circuit to ensure the stability of the design.

Secondly, the design, manufacture and testing of a bidirectional non-isolated current-regulated switched-mode inverter is required to interface a commercially available 3-phase asynchronous machine to a dc bus. A bidirectional transfer of up to 2 kW electrical power between a 3-phase asynchronous machine and a nominally 350 V dc bus is to be demonstrated. The shaft of the inverter-connected asynchronous machine will be coupled to an identical 3-phase asynchronous machine controlled by an off-the-shelf variable-speed drive (VSD) to function as the air-driven turbine. Low-speed commercially available 3-phase asynchronous machines (400 V AC, 3 kW, 3000 rpm) will be employed. A closed-loop control circuit will be designed and analysed to ensure the closed-loop stability of the design. Table 1.1 shows a summary of the system parameters.

The last objective is to integrate and test the inverter, dc bus and dc-dc converter interface. A bidirectional transfer of up to 2 kW of electrical power between the inverter, converter and the load is to be demonstrated. The battery current due to the 2 kW load at the output of the dc-dc converter

Table 1.1: Bidirectional interface system parameters

Parameter	Value
System power rating (bidirectional)	2 kW
DC bus voltage operating range	340 V - 360 V
Nominal dc bus voltage	350 V
Machine speed rating	3000 rpm
Machine power rating	3 kW
Machine voltage rating	400 V AC

should be shown to progressively decrease to zero as the mechanical power applied to the shaft of the inverter-connected machine is progressively raised, until such point as the power delivered by the inverter (less losses) equals that consumed by the load. Similarly, the battery current should be shown to further decrease (below zero) as the mechanical power applied to the shaft of the inverter-connected machine is progressively raised beyond that consumed by the load. Thus, the batteries should discharge while the batteries source power to all or a fraction of the load's requirement, and should charge while the asynchronous machine sources power in excess of that consumed by the load.

1.3 Thesis Outline

The structure of the thesis is briefly described below in terms of the content provided in each of the chapters.

Chapter 2 provides background information on the relevant literature used in this thesis. Previous work regarding the use of ram air turbines as generators is discussed. Bidirectional converter and inverter topologies are investigated along with pulse-width modulation schemes that can be used to control these circuits. The operation and development of an equivalent circuit for an asynchronous machine are also presented.

Chapter 3 describes the basic circuit operation of the bidirectional dc-dc converter circuit. A detailed design of the control circuit used for the converter is presented along with the frequency domain closed-loop stability analysis of the system.

Chapter 4 presents the time domain analysis of the dc-dc converter. The simulation results are compared to the measured results of the prototype circuit, which was manufactured from the specifications given in Chapter 3.

Chapter 5 derives the asynchronous machine parameters from the equivalent machine model and the datasheet information. The machine model is simulated and the results are compared to the given datasheet information in order to confirm the credibility of the model. The generator operation of the

machine is also investigated.

Chapter 6 describes the basic circuit operation of the inverter functioning as a synchronous rectifier. A detailed design of the control loops used to control the inverter switching action is presented. Frequency domain analysis is used to confirm the closed-loop stability of the system. The implementation of additional safety features is discussed.

Chapter 7 details the integration of the inverter and dc-dc converter circuit. The time domain simulation of the inverter circuit is compared with the measured results from the prototype circuit. The dc-dc converter's bidirectional capability is investigated. The test results used to confirm the successful integration between the converter and inverter circuits are presented. Lastly, the safety features' testing procedures and results are given.

Chapter 8 concludes the thesis by presenting the overall system simulation and test results. Future work and recommendations are also considered.

Chapter 2

Literature Review

This literature review gives background information on some of the key elements of the proposed project. The focus is on the use of ram air turbines as generators, the development of converter and inverter circuits and the modelling and operation of three-phase asynchronous machines.

2.1 Ram Air Turbines as Generators

Ram air turbine systems are most commonly used to supply emergency power on-board aircraft when the main power supply fails but can also be used to supply continuous power whilst airborne. The turbine usually drives an electric generator connected to a dc bus and is supported by a battery or other storage device to form a hybrid system [1]. Some of the key requirements of such a system include high reliability, adequate load regulation and high overall system efficiency.

2.1.1 Energy Management Strategies

Since the RAT speed will vary during flight, controlled converters are generally required. These converters operate either to form a controlled interface between the machine and the supply bus, or to regulate the machine excitation, or both [2]. In [1] and [3] two energy management strategies are investigated to interface a RAT and a storage device: the conventional strategy and a dual strategy.

The conventional strategy makes use of a current-controlled dc-dc converter to interface the dc bus and the storage unit. The RAT is used as a voltage source and the excitation current of the generator is controlled to maintain a constant dc bus voltage at the output of the rectifier. The RAT is thus only used to supply the required average power to the load while the storage unit supplies peak and transient power.

In the dual-control strategy, the RAT's generator excitation voltage is controlled in order to regulate the current supplied to the dc bus, while the storage device with its dc-dc converter is used to regulate the dc bus voltage. This allows the use of maximum power point tracking (MPPT) but only if the power demanded by the load and storage device exceeds the maximum power that can be supplied by the RAT. MPPT techniques are explained in detail in [4, 5, 6]. The overall objective is to provide the optimal rotor speed with respect to the ratio between the blade-tip speed and wind speed [7]. This will produce the maximum amount of machine torque and power. The dual strategy optimises energy transfer and is therefore the preferred control strategy.

MPPT is very popular in wind-power applications where the power delivered by wind-driven generators are fed back into a grid or other storage unit with a large storage capacity. In the case of a ram air turbine, the RAT is only used to supply the power required by the load and to charge the storage device to its recommended capacity. Thereafter, no more power must be delivered to the system since there is no place to dump the excess power. If MPPT is used in RAT applications, the system must be designed such that it will exit MPPT mode if the load power requirement is less than the RAT's maximum power.

2.1.2 Existing Power Generation Topologies

Various approaches have been investigated to generate power from a ram air turbine and is summarised in this subsection. In 2005 P.H. Mellor published a paper [8] on generating power from a RAT using a brushless permanent-magnet (PM) generator and an integrated fixed-ratio gearbox. The machine was controlled to produce optimal torque at low speeds, while at high speeds the peak line voltage was limited to the desired dc bus voltage. A resolver to measure the degrees of shaft rotation was used for feedback along with machine current measurements. An insulated-gate bipolar transistor (IGBT) module and a digital signal processor (DSP) based controller was used to control the generator. This design showed an overall system efficiency of 84 %.

A different approach was used by P. Bolognesi in [2] where the generator for the RAT was a hybrid-excited dc machine consisting of both permanent magnets and field coils. The armature of the dc machine is directly connected to the dc bus, while the excitations of the field coils are controlled by means of a chopper circuit to keep the dc bus voltage within the desired voltage range. Extensive modelling showed the validity of such a system.

In [1] the use of a hybrid system comprising of supercapacitors and a synchronous generator are proposed to generate power on board an aircraft. A bidirectional current-controlled dc-dc converter is used to interface with the dc bus and supercapacitors. To reduce current ripple and increase the apparent switching frequency, an interleaved converter was used consisting of two IGBT modules with triple buck-boost branches where the PWM signals

for each branch are 120 degrees phase shifted. Proportional-integral controllers are used to regulate the dc bus voltage. The stator currents of the synchronous generator are rectified through a three-phase diode-bridge rectifier to produce power to the load. Both the conventional and dual energy-management strategies were tested and shown to have nearly equivalent dynamic behaviour.

Similar work was done by X. Roboam in [3] with a bigger focus on the difference between the two energy management strategies. The only difference was shown to be that the dual strategy allows faster dc bus regulation and maintains better system stability during transient operation.

A lithium-ion battery and RAT interface is presented in [9]. The turbine is connected to a synchronous generator through a speed multiplier. A diode rectifier, connected to the dc bus, is used to rectify the three-phase stator voltages. A bidirectional dc-dc converter is used for interfacing the dc bus and Li-Ion battery. Again, both the conventional and dual strategies were tested. The dc bus voltage ripple on the conventional strategy was shown to be less than for the dual strategy, while the dual strategy showed slightly better dc bus regulation.

2.2 DC-DC Converters

The proposed circuit for this thesis requires a switched-mode bidirectional dc-dc converter to interface with the dc bus and battery storage device. The intention is to control the converter current in order to regulate the dc bus voltage. In switched-mode converters this is achieved by controlling the on and off time of the switches. Different switching schemes exist but the most widely used scheme is pulse-width modulation [10] which employs switching at a constant frequency.

2.2.1 Pulse-Width Modulation

Pulse-width modulation (PWM) varies the duty cycle of converter's switches at a high frequency to obtain the desired average output voltage or current [10]. An example of a circuit that uses PWM to control the switches is shown in Fig. 2.1, where insulated-gate bipolar transistors (IGBTs) are used as the switches. The signal to determine the state of a switch (on or off) is obtained by comparing the control signal to a repetitive waveform with a constant frequency, referred to as the carrier waveform as shown in Fig. 2.2. The carrier waveform can either be a sawtooth or triangular waveform [10]. The difference between the desired and actual output is passed through a compensation amplifier to generate the required control signal [11].

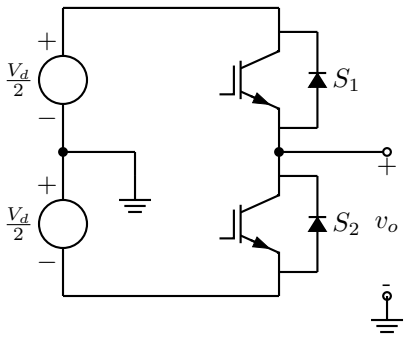

Figure 2.1: Half-bridge converter circuit.

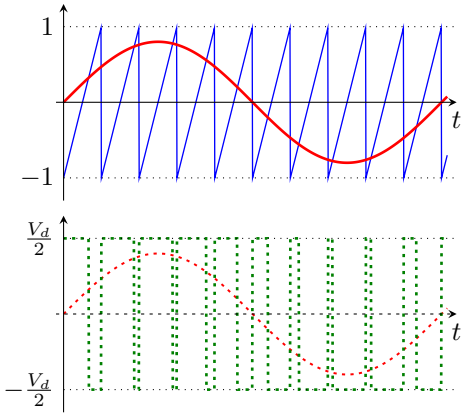

Figure 2.2: PWM signal (green line) generated using a control signal (red line) and sawtooth carrier waveform (blue line).

The duty cycle of a switch with constant control signal $v_{control}$ is expressed by

$$D = \frac{t_{on}}{T_s} = \frac{v_{control}}{\hat{V}_c}, \tag{2.1}$$

where T_s is the switching period which corresponds to the carrier waveform frequency and $\hat{V}_c$ is the peak value of said carrier waveform.

PWM strategies can be divided between naturally sampled PWM and regular sampled PWM. Naturally sampled PWM is the earliest and most straightforward strategy which compares a low-frequency control signal to a high-frequency carrier waveform and is used in analog controllers, as shown in Fig. 2.2. Regular sampled PWM is used in digital control systems where the control signal is sampled at a regular interval and the duty cycle is adjusted in proportion to the value of the sample.

2.2.2 Bidirectional Converter Topology

An in-depth study on the different switched-mode dc-dc converter topologies are given in [12]. For a bidirectional converter the most commonly used topology consists of a half-bridge circuit that can either sink or source current from or to the dc bus [13], [14]. A simple bidirectional half-bridge circuit is shown in Fig. 2.3 with metal-oxide-semiconductor field-effect transistors (MOSFETs) as switches. Alternatively, IGBTs can be used as switches and should include freewheeling diodes across them.

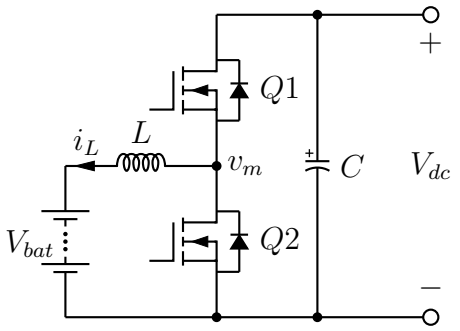

Figure 2.3: Bidirectional dc-dc converter circuit.

From first principles it is known that the average voltage across an inductor under steady state conditions must equal zero [11]. Thus, the following statement with respect to Fig. 2.3 can be made:

$$V_{bat} = \overline{v_m}, \tag{2.2}$$

where $\overline{v_m}$ is the average mid-point voltage which can be calculated as

$$\overline{v_m} = \left(\frac{t_{1(on)}}{T_s} V_{dc} + \frac{t_{2(on)}}{T_s} 0 \right), \tag{2.3}$$

where $t_{1(on)}$ and $t_{2(on)}$ is the on-time of switches Q_1 and Q_2, respectively. From (2.2) and (2.3) the relationship between the dc bus voltage and the battery voltage is thus

$$V_{dc} = \frac{V_{bat}}{\frac{t_{1(on)}}{T_s}} = \frac{V_{bat}}{D_1}, \tag{2.4}$$

where D_1 is the duty cycle of Q_1. The duty cycle of Q_2 is

$$D_2 = \frac{t_{2on}}{T_s} = 1 - D_1 = 1 - \frac{V_{bat}}{V_{dc}}, \tag{2.5}$$

such that Q_1 and Q_2 is never on simultaneously. For ideal switches the above equation would suffice to prevent short-circuit conditions. However, in real

life switches require a finite amount of time to change state. By introducing dead-time, cross conduction can be avoided. The dead-time inserts a small time delay before a switch is turned on in order to allow the other switch to completely switch off first [15].

2.3 DC-AC Inverters

For the proposed project a bidirectional three-phase switched-mode ac-dc inverter circuit is required to interface an asynchronous generator and dc bus. Two topologies exist for inverter circuits, namely current source inverters (CSIs) and voltage source inverters (VSIs). CSIs are only used in very high power applications. For this literature review only VSIs will be considered since they are by far the most commonly used inverter topology [11].

2.3.1 Three-Phase Inverters

The basic topological structure of an inverter circuit is a half-bridge. A three-phase inverter requires three half-bridges where each half-bridge pole-point connects to one of the output load terminals as shown in Fig. 2.4. The switches can either be IGBTs with freewheeling diodes or MOSFETs with built-in diodes to support bidirectional power flow [15].

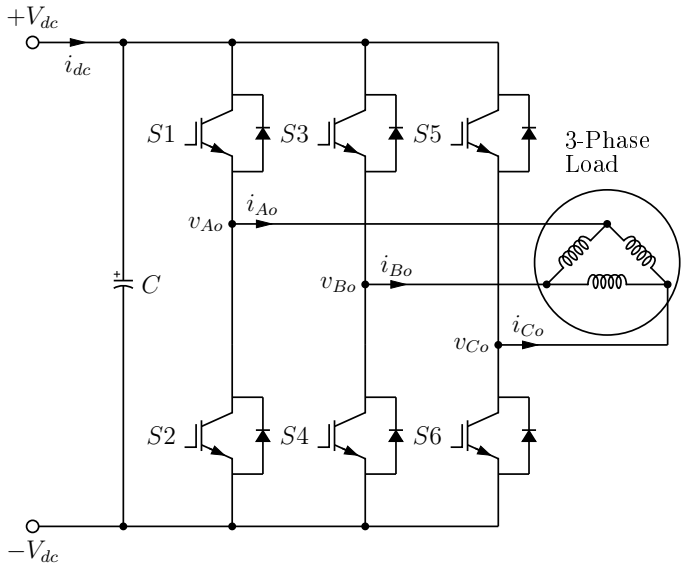

Figure 2.4: Three-phase voltage source inverter connected to a three-phase load.

The principle of operation is similar to that of the circuit described in Section 2.2.2 where the top and bottom switch of each phase leg are switched com-

plementary to each other. Considering the half-bridge circuit with switches S_1 and S_2, when S_1 is switched on the pole voltage v_{Ao} gets pulled high to $+V_{dc}$ and when S_2 is on v_{Ao} gets pulled down to $-V_{dc}$. By controlling the on-time of the switches the fundamental voltage across the load terminals can be controlled. A PWM technique is thus generally also used in VSI circuits to control the switches [16].

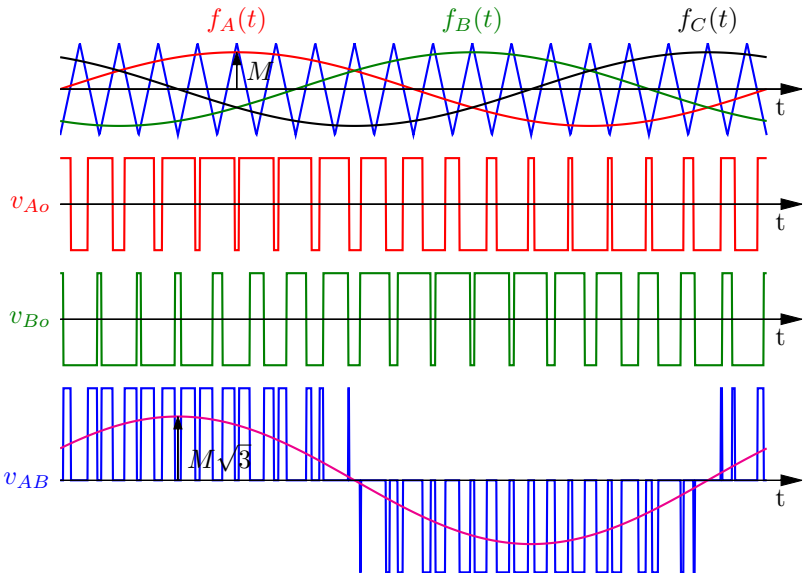

Figure 2.5: PWM voltages generated in three-phase inverter applications.

Three-phase PWM is described in Figure 2.5. It shows three control sinusoids $f_A(t)$, $f_B(t)$ and $f_C(t)$ indicated in red, green and black respectively, where each waveform is controlling one half-bridge. The three waveforms are phase shifted by 120 degrees relative to each other to generate the required fundamental three-phase voltage waveforms at the load terminals. A triangular waveform is used as the carrier waveform and is indicated in blue. The two PWM voltage waveforms v_{Ao} and v_{Bo} represent the two pole voltages from Fig. 2.4, respectively. If the load is connected in delta configuration, the voltage applied across one of the three load windings will equal the difference between the two inverter pole voltages v_{Ao} and v_{Bo}. The resulting PWM waveform is shown as v_{AB} in Fig 2.5. If v_{AB} is put through a low pass filter the resulting waveform is a sinusoid with a amplitude $\sqrt{3}$ times greater than that of the fundamental pole voltage waveforms indicated in Fig 2.5.

The required dead-time to prevent a short-circuit between the dc bus rails varies with the power rating of the inverter circuit. Typically the required dead-time to ensure safe operating conditions is well below 1 μs [15].

2.3.2 Inverter Control Schemes

VSIs can be classified as either current- or voltage-controlled. A CCVSI has the advantage of inherent overcurrent protection.

Three main control schemes exist for inverters that drive ac machines namely scalar control, vector control and direct torque control [17]. Scalar control techniques have been widely used in industry and are easy to implement [16]. Volt/Hertz control is a scalar control technique where the ratio between the stator voltage and frequency is kept constant to ensure a constant air gap flux close to rated flux [18]. Volt/Hertz control is thus used in voltage-controlled voltage-source inverters (VCVSIs). Scalar control gives inferior performance compared to vector control schemes in terms of their speed response. However, if the speed of the machine is not required to change rapidly, scalar control provides more than adequate performance [18].

Vector control allows an ac machine to be controlled as if it were a separately excited dc motor by transforming its phase currents into a synchronously rotating reference frame [19]. The two resulting currents are dc currents, one representing the torque producing component of the stator current while the other corresponds to the flux producing component of the stator current. By controlling these two currents the machine flux and torque can thus be controlled. Vector control, also known as field-oriented control, provides excellent performance but with the drawback of high complexity. Vector control schemes require a powerful microcontroller or DSP [16]. With vector control the inner control loop is always current controlled allowing it to function as a CCVSI. Different forms of field-oriented control (FOC) exist such as indirect FOC [20] and direct FOC [21], [22].

Direct torque control (DTC) schemes control both the torque and stator flux of the machine whereby the required flux and torque is compared to the respective estimated values to generate two error voltages. The error voltages are constrained to lie between an upper and lower limit respectively, thus providing hysteresis-band control [23]. A detailed description of DTC is given in [17]. Direct torque control schemes have shown similar performance to that of vector control schemes [16]. The combination of DTC and vector control schemes also exist and is presented in [24].

2.4 Asynchronous Machines

This project will make use of two asynchronous machines, one to function as a generator, the other to drive the shaft of the generator. The operation of asynchronous machines is investigated in order to model and develop the control circuit for the inverter controlling the generator.

2.4.1 Principle of Operation

Asynchronous machines, also known as induction machines, are the most commonly used type of ac machines in industry. The machine consists of a stator and rotor winding that are magnetically coupled to transfer energy between mechanical and electrical systems [19]. The rotor of an induction machine can be classified as either a wound rotor or a squirrel-cage rotor. Wound rotor induction machines are fairly uncommon, thus for this study only squirrel-cage rotor induction machines are investigated. A squirrel-cage rotor is constructed such that the windings on the rotor are conducting bars short-circuited at each end by conducting rings. Both the stator and rotor cores are made from laminated ferromagnetic material.

The fundamental principle of induction machines is that of a rotating sinusoidally-distributed magnetic field within the air gap of the machine. This is achieved by applying balanced sinusoidal three-phase voltages to the stator windings and in return a synchronously rotating magnetic field is produced. A summary of the analytical derivation [16] follows below.

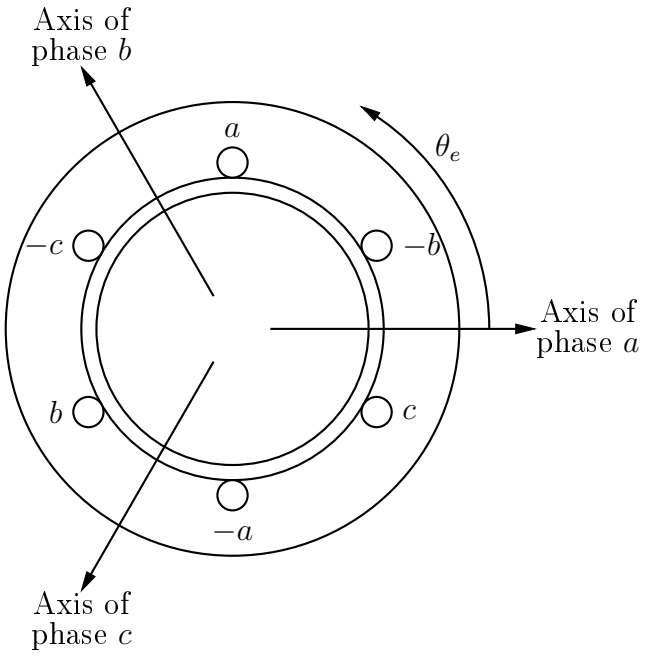

Figure 2.6: Ideal three-phase, two pole induction machine.

Figure 2.6 shows an ideal three-phase, two-pole induction machine where the phase windings for the stator are indicated by concentric circular coils. The machine can either be connected in delta or wye configuration. The three-phase windings are 120 degrees displaced from each other (sinusoidally distributed) and the air gap in the machine is considered uniform.

When balanced sinusoidal three-phase voltages are applied to the windings the instantaneous currents are

$$i_a = I_{\max}\cos(\omega_e t), \tag{2.6}$$

$$i_b = I_{\max}\cos(\omega_e t - 120°), \tag{2.7}$$

$$i_c = I_{\max}\cos(\omega_e t + 120°), \tag{2.8}$$

where I_{max} is the maximum stator winding current, $\omega_e t$ is the frequency of the applied excitation voltage and t denotes time. Each of the phase windings will independently induce a sinusoidally distributed magnetomotive force (mmf) wave since

$$\mathcal{F} = Ni, \tag{2.9}$$

where $\mathcal{F}$ is mmf and N is the number of turns in a phase winding. The resulting mmf expressions are given by

$$\mathcal{F}_a = Ni_a\cos(\theta), \tag{2.10}$$

$$\mathcal{F}_b = Ni_b\cos(\theta - 120°), \tag{2.11}$$

$$\mathcal{F}_c = Ni_c\cos(\theta + 120°), \tag{2.12}$$

where θ is the spatial angle. The total mmf at angle θ is given as

$$\begin{aligned}\mathcal{F}(\theta) &= \mathcal{F}_a(\theta) + \mathcal{F}_b(\theta) + \mathcal{F}_c(\theta) \\ &= Ni_a\cos(\theta) + Ni_b\cos(\theta - 120°) + Ni_c\cos(\theta + 120°).\end{aligned} \tag{2.13}$$

Substituting (2.6) through (2.8) in (2.13) results in

$$\begin{aligned}\mathcal{F}(\theta, t) = NI_{\max}\,[&\cos(\omega_e t)\cos(\theta) + \cos(\omega_e t - 120°)\cos(\theta - 120°) \\ &+ \cos(\omega_e t + 120°)\cos(\theta + 120°)]\,.\end{aligned} \tag{2.14}$$

After simplifying (2.14) the expression becomes

$$\mathcal{F}(\theta, t) = \frac{3}{2}NI_{\max}\cos(\omega_e t - \theta). \tag{2.15}$$

The air gap mmf wave from (2.15) is shown to be sinusoidally distributed, rotating at synchronous speed ω_s where

$$\omega_s = \frac{2}{\text{poles}}\omega_e. \tag{2.16}$$

For a two-pole machine the angular frequency of the applied electrical excitation ω_e is equal to the synchronous speed of the air gap mmf ω_s. In revolutions per minute the synchronous speed can be expressed by

$$n_s = \left(\frac{120}{\text{poles}}\right) f_e, \tag{2.17}$$

since

$$f_e = \frac{\omega_e}{2\pi}, \tag{2.18}$$

where f_e is the applied electrical frequency. The time-varying mmf wave will produce an electric field in accordance with Faraday's law:

$$\oint_c \mathbf{E} \cdot \mathbf{ds} = -\frac{d}{dt} \int_S \mathbf{B} \cdot \mathbf{da}. \tag{2.19}$$

Equation (2.19) states that the induced electromotive force (emf) around a closed contour is equal to the negative rate of change of the magnetic flux ϕ passing through an enclosed area [25] since

$$\phi = \int_S \mathbf{B} \cdot \mathbf{da}. \tag{2.20}$$

The rotor winding forms the closed contour and links the core flux N times, thus (2.19) reduces to

$$e = -N\frac{d\phi}{dt} = -\frac{d\lambda}{dt}, \tag{2.21}$$

where λ is the flux linkage of the winding. The emf e will cause an induced current to flow in the rotor winding. When the current-carrying winding is exposed to a magnetic field, torque is produced to rotate the rotor winding. This is referred to as the starting torque. If the torque on the load attached to the shaft of the motor is less than the starting torque, the rotor will start to turn [16]. The rotor will turn in the same direction as that of the rotating mmf wave in accordance with Lenz's law, which states that an induced emf produces a current that will flow in the direction to oppose the change which produced it [25].

If the rotor were to rotate at synchronous speed, no induction would take place and hence no torque would be produced. At any other speed, rotor current is induced and asynchronous torque is developed, hence the name asynchronous machine. The difference between the synchronous speed n_s and the rotor shaft speed n_r is called the slip speed and is commonly referred to as the slip of the motor. Slip s in per unit is

$$s = \frac{n_s - n_r}{n_s} = \frac{\omega_s - \omega_r}{\omega_s} = \frac{\omega_{sl}}{\omega_s}, \tag{2.22}$$

where ω_{sl} is the slip frequency. Slip is generally expressed as a percentage of the synchronous speed. From (2.22) the rotor speed is

$$n_r = (1 - s)n_s, \tag{2.23}$$

or

$$\omega_r = (1 - s)\omega_s. \tag{2.24}$$

While the rotor is stationary, the slip is 1 per unit and the rotor now behaves the same as a secondary winding on a transformer. The rotor frequency is the same as the stator frequency until the rotor starts to turn. The relative motion between the stator flux and rotor is responsible for the induced emf in the rotor windings and the frequency of the induced emf in the rotor is

$$f_r = sf_e, \tag{2.25}$$

where f_e is the electrical frequency of the applied currents in the stator. If the per unit slip value is between 1 and 0 the asynchronous machine is operated as a motor and hence electrical power is converted to mechanical power. From (2.24) a per unit slip value smaller than 0 indicates the rotor shaft speed is greater than the synchronous stator speed. To achieve this, torque has to be applied to the shaft of the induction machine and thus the induction machine now functions as a generator. The stator terminals are then used as a voltage source to supply electrical power [26]. Applications include the use of an induction generator driven by a wind turbine and connected to a power system to provide renewable energy. This thesis will use an induction machine operated at negative slip in order to supply power to a load.

2.4.2 Equivalent Circuit

A transformer functions by transferring power exclusively to windings through induction. An induction machine can thus be seen as a transformer with a rotating secondary winding [27]. Due to the similarity between induction machines and transformers, the model of an induction machine is similar to that of a transformer. A single-phase equivalent circuit of a squirrel-cage induction motor is shown in Fig. 2.7.

The stator side is modelled as an inductor L_{ls} in series with a resistor R_s to represent the leakage impedance. The air gap model consists of two shunt components, a core-loss resistance R_c and a magnetizing inductance L_m. Induction machines are usually operated at low slip and hence the frequency of the induced rotor emf is also low. Due to this, the core loss of the rotor magnetic circuit is often ignored [27]. The rotor is modelled as leakage inductance L_{lr} in series with rotor resistance R_r. The rotor quantities are however referred to the stator side assuming a turns ratio of 1:1. The impedance of the rotor referred to the stator is

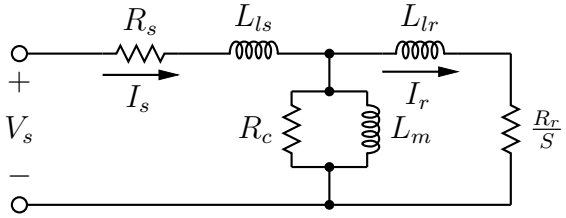

Figure 2.7: Single-phase equivalent circuit of an induction motor.

$$Z_r = R_r + j\omega_{sl}L_{lr}. \tag{2.26}$$

After substituting (2.22) in the above equation and simplifying, (2.26) becomes

$$Z_r = \frac{R_r}{s} + j\omega_s L_{lr}. \tag{2.27}$$

The rotor reactance is now defined in terms of the stator frequency and can be analysed as part of the stator equivalent circuit as shown in Fig. 2.7.

From the equivalent circuit the necessary power equations can be determined. For a three-phase motor the input power is

$$P_{in} = 3V_s I_s \cos(\theta), \tag{2.28}$$

where θ is the phase difference between the applied stator voltage V_s and the current I_s flowing through the stator winding. The stator winding copper loss is

$$P_{stator} = 3{I_s}^2 R_s. \tag{2.29}$$

The power transferred across the air gap is

$$P_{gap} = \frac{3{I_r}^2 R_r}{s}. \tag{2.30}$$

The rotor copper loss is

$$P_{rotor} = 3{I_r}^2 R_r. \tag{2.31}$$

The electromechanical power developed by the motor is thus

$$P_{mech} = P_{gap} - P_{rotor} = 3{I_r}^2 R_r \left(\frac{1-s}{s}\right) = (1-s)P_{gap}. \tag{2.32}$$

The electromechanical torque produced can be calculated since mechanical power is equal to angular velocity times torque [26]. With reference to (2.24) the mechanical torque expression becomes

$$T_{mech} = \frac{P_{mech}}{\omega_r} = \frac{P_{gap}}{\omega_s} = 3{I_r}^2 \frac{R_r}{s\omega_s}. \tag{2.33}$$

The current flowing in the rotor is thus responsible for creating the required motor torque. The torque applied to the shaft of the motor will equal the mechanical torque minus the friction, windage and other rotational losses. This equivalent circuit and derived equations of an induction machine can be used to model and predict the behaviour of induction machines.

2.4.3 Dynamic d-q Model

For a dynamic model of a three-phase machine, three equivalent circuits are required, one for each phase. In order to simplify and reduce the total number of differential equations, a variable transformation first formulated by R.H. Park in the 1920's can be applied to the equivalent circuit. The Park transformation refers stator variables to a synchronously rotating reference frame with respect to the rotor. The transformation has since been generalised such that machine variables are referred to a frame of reference that is rotating at an arbitrary angular velocity. The preferred transformation to analyse the dynamic behaviour of a balanced three phase machine is where both the stator and rotor variables are transformed to a synchronously rotating $dq0$ reference frame that turns with the rotating magnetic field. This transformation turns the voltage and current ac quantities into dc quantities allowing better analysis of the machine's transient responses [19].

The $dq0$ transformation transforms the three-phase abc system into two rotating components, namely the direct (d) and quadrature (q) axis. The q-axis is aligned with the a-axis and precedes the d-axis by 90°. A third component, the zero-sequence component, is also included to complete the transformation of the three phase variables. However, under balanced three phase conditions, no zero-sequence components are present [26]. The formulation of the $dq0$ transform is explained in [28] and is given by

$$\boldsymbol{\xi}_{qd0} = \mathbf{K}(\phi)\boldsymbol{\xi}_{abc}, \tag{2.34}$$

where

$$\mathbf{K}(\phi) = \frac{2}{3}\begin{bmatrix} \cos\phi & \cos(\phi - \frac{2\pi}{3}) & \cos(\phi + \frac{2\pi}{3}) \\ \sin\phi & \sin(\phi - \frac{2\pi}{3}) & \sin(\phi + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}. \tag{2.35}$$

The inverse $dq0$ transform is used to transform the variables back to the abc reference frame and is given by

$$\boldsymbol{\xi}_{abc} = \mathbf{K}^{-1}(\phi)\boldsymbol{\xi}_{qd0}, \tag{2.36}$$

where

$$\mathbf{K}^{-1}(\phi) = \begin{bmatrix} \cos\phi & \sin\phi & 1 \\ \cos(\phi - \frac{2\pi}{3}) & \sin(\phi - \frac{2\pi}{3}) & 1 \\ \cos(\phi + \frac{2\pi}{3}) & \sin(\phi + \frac{2\pi}{3}) & 1 \end{bmatrix}. \tag{2.37}$$

The angle ϕ is equal to $\omega_e t$ for the synchronously rotating reference frame where all variables are referred to the stator side.

The dynamic d-q model [29] of the equivalent circuit analysed in Section 2.4.2 is shown in Fig. 2.8. The core-loss resistance is omitted for this model. Note, the rotor side is short-circuited as would be the case for a squirrel-cage induction machine.

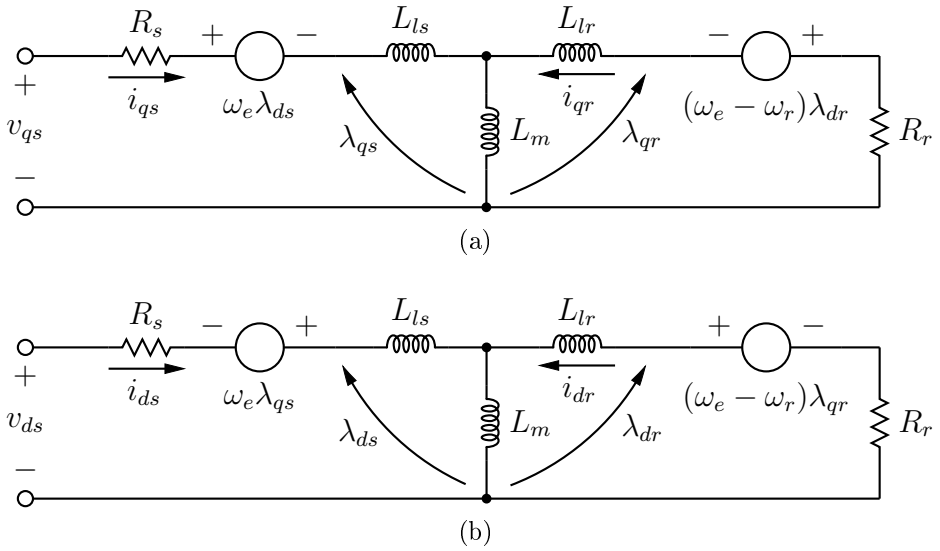

Figure 2.8: Dynamic d-q model of a squirrel cage induction motor for the (a) q-axis component and (b) d-axis component.

From Fig. 2.8 the following differential equations can be deduced:

$$v_{qs} = R_s i_{qs} + \frac{d}{dt}\lambda_{qs} + \omega_e \lambda_{ds}, \tag{2.38}$$

$$v_{ds} = R_s i_{ds} + \frac{d}{dt}\lambda_{ds} - \omega_e \lambda_{qs}, \tag{2.39}$$

$$v_{qr} = 0 = R_r i_{qr} + \frac{d}{dt}\lambda_{qr} + (\omega_e - \omega_r)\lambda_{dr}, \tag{2.40}$$

$$v_{dr} = 0 = R_r i_{dr} + \frac{d}{dt}\lambda_{dr} - (\omega_e - \omega_r)\lambda_{qr}, \tag{2.41}$$

where the flux linkages can be written as:

$$\lambda_{qs} = L_{ls} i_{qs} + L_m (i_{qs} + i_{qr}), \tag{2.42}$$

$$\lambda_{ds} = L_{ls} i_{ds} + L_m (i_{ds} + i_{dr}), \tag{2.43}$$

$$\lambda_{qr} = L_{lr} i_{qr} + L_m (i_{qs} + i_{qr}), \tag{2.44}$$

$$\lambda_{dr} = L_{lr} i_{dr} + L_m (i_{ds} + i_{dr}). \tag{2.45}$$

From [16] the derived torque expression for the developed motor torque in d-q form becomes:

$$T_e = \frac{3}{2} L_m (i_{qs} i_{dr} - i_{ds} i_{qr}). \tag{2.46}$$

In variable frequency applications the rotor speed ω_r is not a constant and can be related to the torque by

$$T_e = T_L + J \frac{d\omega_r}{dt}, \tag{2.47}$$

where T_L is the load torque and J is the rotor inertia.

Equations (2.38) to (2.47) provide the complete model of an induction machine and will be used for modelling purposes.

2.5 Summary

This chapter gave the foundation of the research covered in this thesis. Previous work regarding the use of ram air turbines as generators was presented. Bidirectional converter and inverter topologies were investigated, along with pulse-width modulation schemes that are used to control both inverter and converter circuits. The operation and development of the equivalent circuit for an asynchronous machine were also presented.

Chapter 3

DC-DC Converter Design and Implementation

This chapter describes the design of a non-isolated bidirectional current-controlled voltage-regulated switched-mode dc-dc converter. To facilitate the regulation of the dc bus voltage, two control loops (an inner and an outer) are employed. A detailed design of the control circuitry is given and the closed-loop stability is investigated. The design of a two-stage soft-start circuit to limit the inrush current from the battery to the dc bus during start-up is presented as well as the design of the gate-drive circuitry.

3.1 Basic Circuit Operation

The dc bus voltage is required to be regulated in the range of 340 V to 360 V (350 V nominal), regardless of the direction of current flow through the battery. The dc bus is divided between a positive (+175 V) and negative (-175 V) rail to achieve a nominal rail-to-rail voltage of 350 V. Each rail section has its own bidirectional converter and is designed to function independently using identical controllers. The chosen converter topology is two bidirectional half-bridge circuits, one on top of the other, as shown in Fig. 3.1 with the midpoint grounded.

Twenty 12 V, 40 Ah rated deep-cycle lead-acid batteries are divided between the two rail sections, each using ten batteries indicated by V_{bat}. Table 3.1 shows the characteristic values of a single BSB DB12-40 battery with a floating life expectancy of 12 years. The internal battery resistance, equivalent series resistance of the inductor and the resistance of the switches are all accounted for by one representative resistor in the converter denoted R_{in} in Fig. 3.1.

For the duration of this thesis small letter variables refer to instantaneous values while capital letter variables refer to average values.

If the average inductor current I_L is positive, current is flowing from the dc bus into the batteries, thus charging the batteries. A negative average induc-

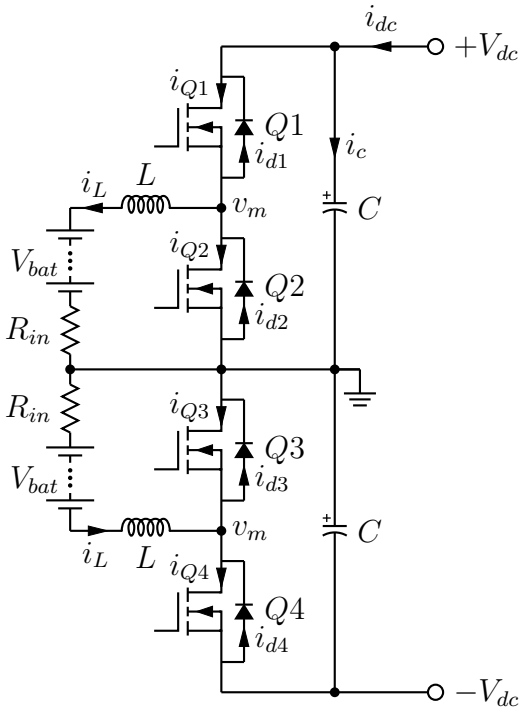

Figure 3.1: Bidirectional dc-dc converter circuit.

Table 3.1: BSB DB12-40 battery specifications.

Parameter	Description	Value
V_b	Rated battery voltage	12 V
Q_{Ah}	Charge capacity	40 Ah
V_{bf}	Maximum float use charge voltage	13.8 V
V_{bc}	Maximum cycle use charge voltage (10 A max)	14.8 V
R_b	Internal resistance at full charge	9.5 mΩ

tor current indicates current flowing from the batteries into a load connected between the dc bus rails. To ensure the 2 kW bidirectional power flow specification is met, the maximum and minimum average inductor current I_L is set to ±10 A corresponding to ±2.4 kW of power at the battery's side of the converter. Also, the recommended maximum charging current of the batteries is given in the datasheet as 10 A.

Discrete MOSFETs are used as the switches for Q_1 through Q_4 and the switching frequency is set to 40 kHz.

With reference to Fig. 3.1, Fig. 3.2 shows the inductor voltage and current for the top-half of the converter circuit when the batteries are being charged at a maximum mean current of 10 A. When switch Q_1 is on (and Q_2 is off) the voltage across the inductor is $v_{L(max)} = V_{dc}$-$V_{bat} = 55$ V. Similarly, when

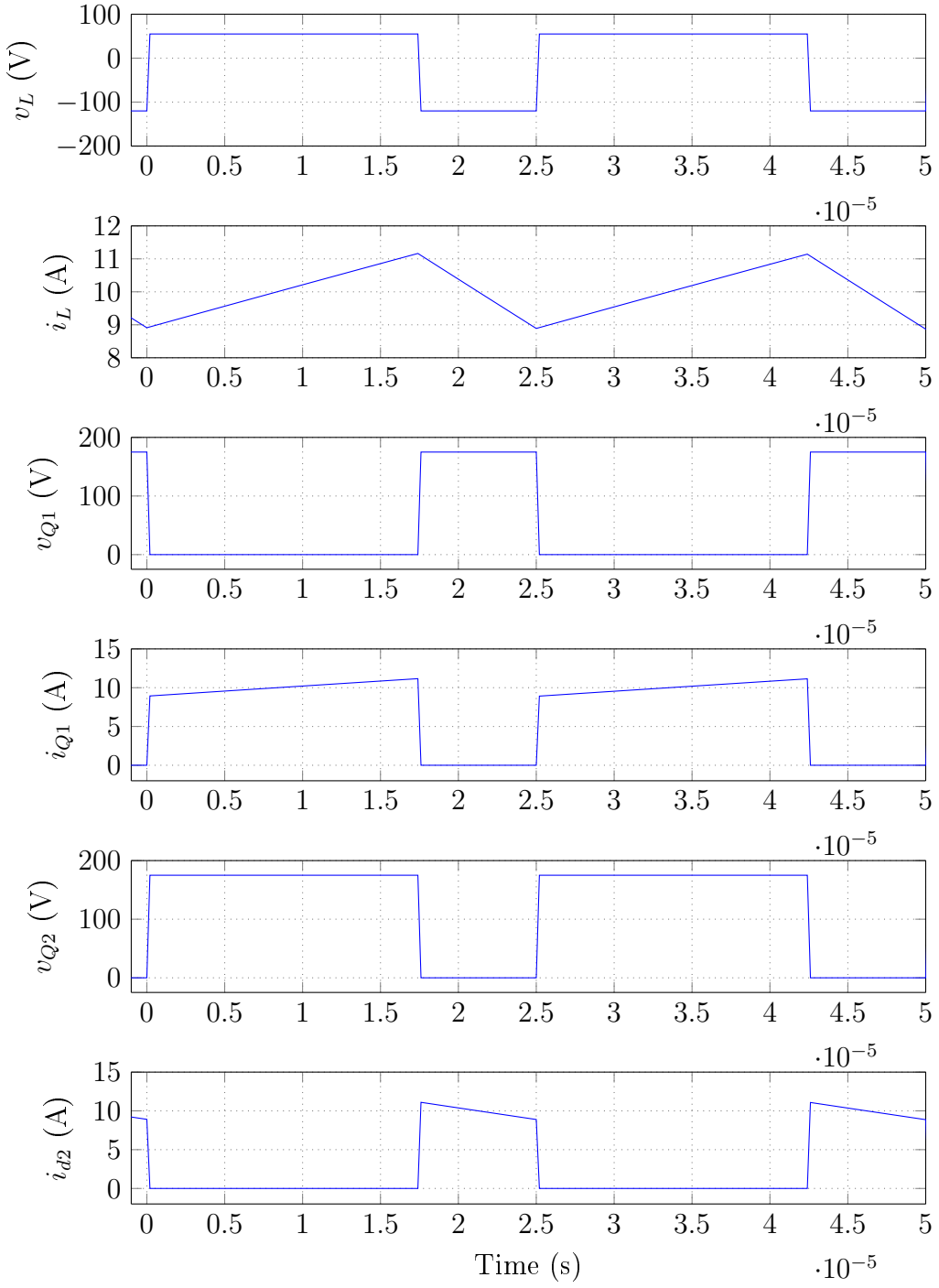

Figure 3.2: Current and voltage waveforms describing the operation of the converter when the batteries are being charged at maximum current.

switch Q_2 is on (and Q_1 is off) the inductor voltage is $v_{L(min)}$ = -V_{bat} = -120 V.

Since

$$v_L = L\frac{di_L}{dt}, \tag{3.1}$$

the inductor current changes linearly with time. However in order that the inductor conduct a current that is on average (typically averaged over 5 to 10 switching cycles) constant, the time averaged voltage applied to the inductor must be zero. That is to say $V_L = 0$. Thus

$$t_{1(on)}(V_{dc} - V_{bat}) + t_{2(on)}(0 - V_{bat}) = 0, \tag{3.2}$$

where $t_{1(on)}$ is the on-time of switch Q_1 and similarly $t_{2(on)}$ is the on-time of switch Q_2. During individual switching cycles, however, the inductor current ramps up linearly through the MOSFET of Q_1 from its minimum value ($i_{L(min)}$) to its maximum value ($i_{L(max)}$) during the on-time of switch Q_1. The on-time of a switch with respect to the total switching period is more commonly referred to as the duty cycle and for Q_1 the duty cycle is

$$D_1 = \frac{t_{1(on)}}{T_s} = \frac{V_{bat}}{V_{dc}} = \frac{120}{175} = 0.6857, \tag{3.3}$$

as derived in Section 2.2.2. Similarly the inductor current ramps down from its maximum to its minimum value during the on-time of Q_2. Thus the duty cycle of Q_2 is given by

$$D_2 = 1 - D_1 = \frac{t_{2(on)}}{T_s} = \frac{V_{dc} - V_{bat}}{V_{dc}} = \frac{55}{175} = 0.3143. \tag{3.4}$$

The voltage across the drain and source of switches Q_1 and Q_2 are shown in Fig. 3.2. Due to the direction of current when the mean inductor current is positive, current can only flow through the MOSFET of Q_1 and through the diode of Q_2. These current waveforms are also shown in Fig. 3.2 where i_{Q1} denotes the MOSFET current through Q_1 and i_{d2} denotes the diode current through Q_2 as indicated in Fig. 3.1.

The bottom-half of the converter will function in a similar manner where the duty cycle of switch Q_4 equals that of Q_1 and the duty cycle for Q_3 is the same as Q_2's. The inductor current and voltage waveforms also remain the same.

If the mean inductor current of 10 A were to change to -10 A, the basic circuit operation stays the same, however current will flow in the opposite direction, thus supplying current to the dc bus. Due to the change of current direction, current will now flow through the diode of Q_1 and through the MOSFET of Q_2 as shown in Fig. 3.1 and Fig. 3.3. The voltage across the inductor and switches will remain the same as before. The duty cycles of the switches also remain the same.

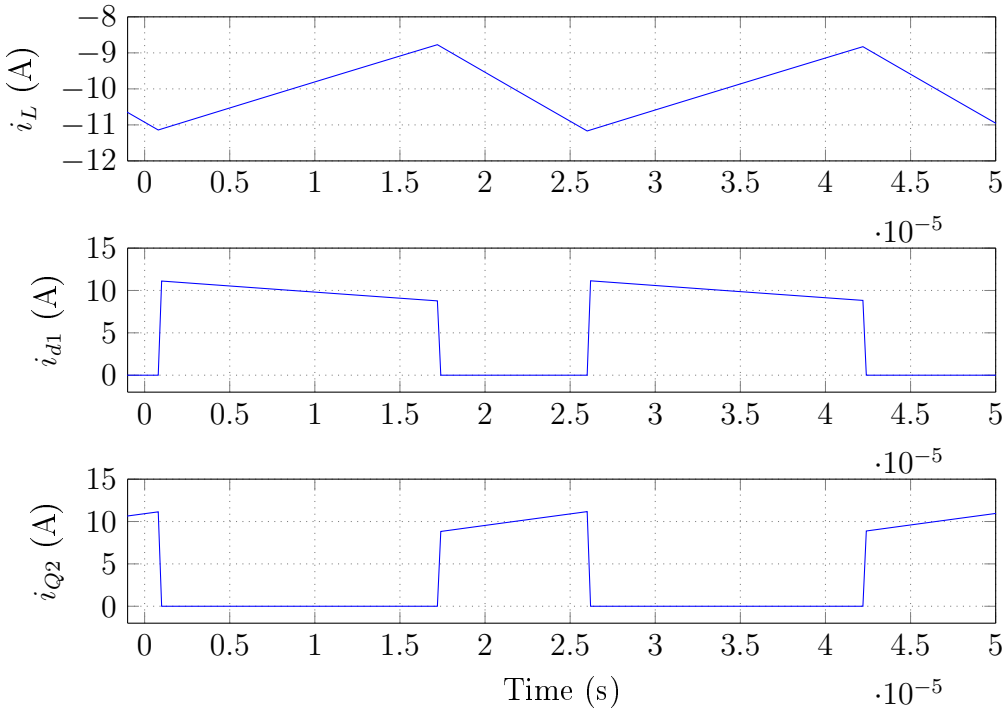

Figure 3.3: Current waveforms describing the operation of the converter when the batteries are sourcing maximum current.

3.1.1 Inductor Design

Both inductors labelled L in Fig. 3.1 are wounded from Litz wire with a 3.8 mm^2 total cross-sectional area (120 strands of 0.2 mm diameter enamelled copper wire) wound over an Arnold A-866142-2 powdered-iron toroidal core. The current density in the wire at a maximum average inductor current of 10 A is 2.65 A/mm^2. The inductor is designed to have a peak-to-peak current ripple of approximately 22.5 % of the absolute maximum value of the mean battery current, thus 2.25 A.

Since the voltage applied across the inductor is constant while either Q_1 or Q_2 is on, then, from (3.1) and (3.2):

$$\begin{aligned} v_L \Delta t &= L \Delta i_L \\ &= v_{L(max)} t_{1(on)} \\ &= -v_{L(min)} t_{2(on)}. \end{aligned} \tag{3.5}$$

Rearranging and substituting (3.3) and (3.4) into the above equation yields

$$\begin{aligned}\Delta i_L &= \frac{v_{L(max)} D_1 T_s}{L} \\ &= -\frac{v_{L(min)} D_2 T_s}{L} \\ &= \frac{37.7 T_s}{L},\end{aligned} \tag{3.6}$$

where $v_{L(max)}$ and $v_{L(max)}$ were already determined as 55 V and -120 V. With a peak-to-peak inductor current ripple of 2.25 A and given that

$$T_s = \frac{1}{f_s} = \frac{1}{40 \text{ kHz}} = 25 \ \mu\text{s}, \tag{3.7}$$

the value of the inductor L is thus calculated from (3.6) and (3.7) as 420 μH. The inductance rating, also known as the A_L value of a core, is used to determine the amount of turns required to achieve a specific inductance for that particular core. The A_L value for the Arnold A-866142-2 core is given in the datasheet as 142 nH/turn^2. The required number of turns is thus:

$$N = \sqrt{\frac{L}{A_L}} = 54.32 \approx 55. \tag{3.8}$$

To ensure the inductor core will not saturate, additional calculation are needed. From Ampere's Law [26] it is known that

$$H_c = \frac{N I_L}{l_e}, \tag{3.9}$$

where H_c is the average magnetic field intensity in the core and l_e is the mean flux path (core) length. Converting (3.9) into Oersted by multiplying with the conversion factor of $\frac{4\pi}{1000}$, results in a magnetic field intensity of

$$H_c = \frac{4\pi N I_L}{1000 \ l_e} = \frac{(0.4)\pi(55)(10)}{19.612} = 35.24 \text{ Oe}. \tag{3.10}$$

The following relationship applies provided the inductor core is not saturated:

$$B_c = \mu H_c, \tag{3.11}$$

where B_c is the magnetic core flux density and μ the permeability given as 125 in the datasheet. The resulting flux density in Kilogauss is thus 4.41 KG. When comparing these values to the datasheet showing the B-H curve of the A-866142-2 core in Oersted and Kilogauss, it can be seen that the core will only saturate for a magnetic field intensity greater than 100 Oe. The magnetic core will thus not saturate for the designed conditions. The B-H curve is however not completely within the linear approximation range of the permeability at this point.

The graph indicates a true flux density of approximately 3.4 KG resulting in a permeability closer to 90 when a mean current of 10 A flows through the

55 core windings which will influence the amount of inductor current ripple. Inductance can also be calculated as [26]

$$L = \frac{N^2 \mu A_c}{l_c}, \tag{3.12}$$

where A_c is the cross-sectional area of the core. From the above equation it can be seen that a decrease in permeability (with all other variables remaining constant) will cause a decrease in inductance. A lower inductance with the same amount of voltage applied across it for the same duration of time will ultimately result in a larger current ripple as deduced from (3.6). The current ripple at a mean inductor current of zero or close to zero will thus have a peak-to-peak value equal to 2.25 A as designed for, however at a mean inductor current of 10 A the inductor ripple will rise to a value closer to 3 A.

3.1.2 Bus Capacitor Design

The assumption is made that the mean current I_{Q1} flowing through switch Q_1 equals the mean dc bus current I_{dc}, which is either sourced by another circuit or sunk by a resistive load connected between the dc bus rails. Thus,

$$I_{dc} = I_{Q1} = I_L D_1, \tag{3.13}$$

where I_L is the average inductor current and D_1 is defined in (3.3). The mean dc bus voltage is assumed constant at 175 V, hence only the ripple component of i_{Q1} flows through capacitor C. At a maximum average inductor current of 10 A, the corresponding currents i_{Q1} and i_c are shown in Fig. 3.4. The capacitor current i_c is negative simply due to the positive reference direction chosen for the current as indicated in Fig 3.1.

By definition current is equal to the rate at which charge flows, hence:

$$i_c = \frac{dq}{dt}, \tag{3.14}$$

where q denotes electric charge. In integral form the above equation becomes

$$q = \int i_c dt. \tag{3.15}$$

From Fig. 3.2 and Fig. 3.3 it can be seen that the maximum magnitude of the capacitor current i_c will remain the same whether the mean inductor current is positive or negative. From (3.15) the net charge Δq, while either switch Q_1 or Q_2 is on, is calculated as the time integral of the capacitor current i_c during that time period. With reference to Fig. 3.4 and while Q_1 is off and Q_2 is on, the net charge is calculated as an area where

$$\Delta q = I_{Q1} D_2 T_s = (I_L D_1) D_2 T_s = 53.88\ \mu C. \tag{3.16}$$

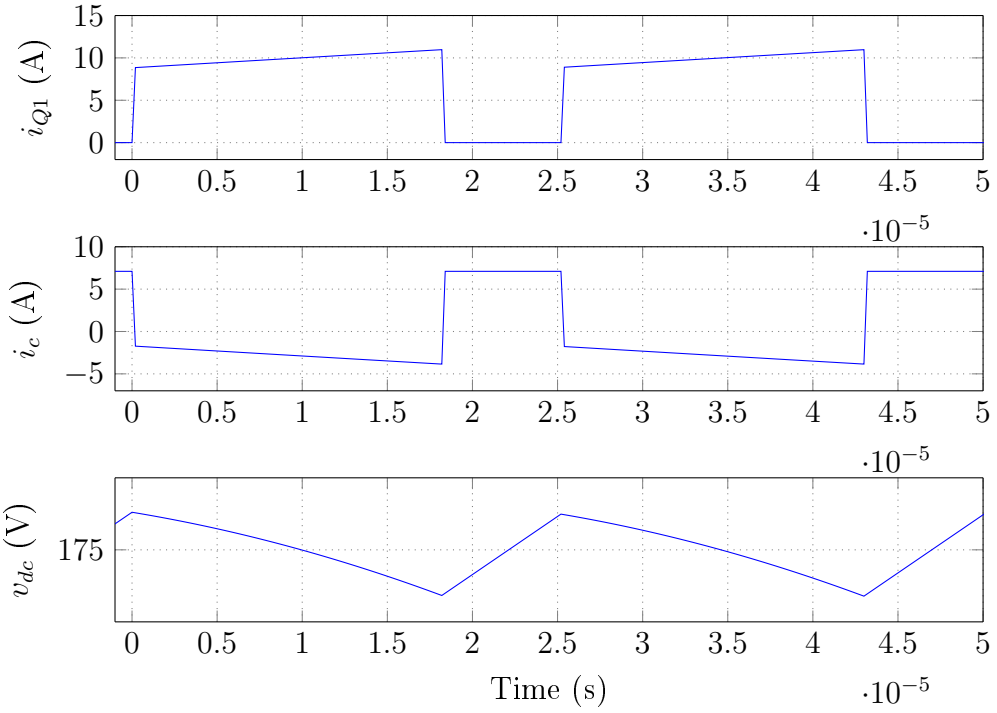

Figure 3.4: Waveforms indicating the capacitor current and voltage when the batteries are being charged at the maximum current.

From first principles it is known that charge is also equal to capacitance times voltage, hence:

$$q = Cv_c, \tag{3.17}$$

where v_c is the voltage across the capacitor. The ripple component on the dc bus voltage is chosen as 30 mV (approximately 0.02 % of the mean dc bus voltage). The value of the capacitor required at the dc bus is thus calculated as 1796 μF from (3.16) and (3.17).

Two parallel connected 1000 μF, 200 V Panasonic electrolytic capacitors were chosen for each of the dc bus capacitors C shown in Fig. 3.1. The resulting voltage ripple on the dc bus as shown in Fig. 3.4 is thus 27 mV. The rms value of the capacitor current i_c shown in Fig. 3.4 was calculated in MATLAB as 4.54 A. Since two parallel connected capacitors are used, the rms current through each of them is 2.27 A. The datasheet gives the maximum operating rms ripple current as 4.85 A for one capacitor. The rms ripple current is thus well within the allowed operating range.

The final component values used in the bidirectional dc-dc converter circuit is given in Table 3.2.

Table 3.2: Converter circuit parameters.

Parameter	Value
V_{dc}	175 V
V_{bat}	120 V
R_{in}	1 Ω
L	419 μH
C	2000 μF

3.1.3 MOSFET Power Loss and Heat Sink Design

The switches used for Q_1 through Q_4 are International Rectifier's IRFP264 MOSFETs. Table 3.3 shows the characteristic values of the chosen MOSFETs.

Table 3.3: IRFP264 MOSFET parameter values.

Parameter	Description	Value
V_{DSS}	Drain-to-source breakdown voltage	250 V
$R_{DS(on)}$	Static drain-to-source on-resistance (V_{GS} = 10 V)	75 mΩ
I_D	Maximum continuous drain current (T_c = 25°)	38 A
Q_g	Maximum total gate charge	210 nC
$t_{c(on)}$	Turn-on (rise) time	99 ns
$t_{c(off)}$	Turn-off (fall) time	92 ns

The calculation of MOSFET power losses for half-bridge topologies are described in detail in [30] and [31] where the diodes are assumed ideal. For the bidirectional dc-dc converter circuit two cases have to be investigated, one for positive inductor current and one for negative inductor current.

CASE 1: Positive Inductor Current

Current can only flow from the dc bus into the batteries when switch Q_1 is closed since the diode in Q_1 is reversed biased. Switching as well as conduction losses are thus present. Due to the direction of the inductor current, current will however flow through the freewheeling diode of Q_2 causing diode losses.

When a MOSFET transitions from on to off and similarly from off to on, there is a small time period ($t_{c(on)}$ and $t_{c(off)}$) during which the switch has a voltage across it as well as a current flowing through it. This results in switching losses. In Fig. 3.2 the current through Q_1 is shown. The absolute maximum and minimum inductor current is 11.125 A ($i_{L(max)}$) and 8.875 A ($i_{L(min)}$) respectively, which corresponds to an average maximum current of 10 A with 2.25 A of ripple. The average switching losses for Q_1 are thus calculated as [31]

$$P_{c(on)} = \frac{1}{2} V_{dc} i_{L(min)} t_{c(on)} f_s, \tag{3.18}$$

and

$$P_{c(off)} = \frac{1}{2} V_{dc} i_{L(max)} t_{c(off)} f_s. \tag{3.19}$$

The total switching losses for Q_1 are thus

$$\begin{aligned} P_{switch} &= \frac{1}{2} V_{dc} f_s \left(i_{L(min)} t_{c(on)} + i_{L(max)} t_{c(off)} \right) \\ &= 6.66 \text{ W}. \end{aligned} \tag{3.20}$$

The conduction losses occur due to the on-resistance of the switches and are given by [31]

$$P_{cond} = R_{DS(on)} I^2_{Q(rms)}. \tag{3.21}$$

When switch Q_1 is turned on the voltage across the inductor changes almost instantaneously from $-V_{bat}$ to $V_{dc} - V_{bat}$ while the current through the inductor rises gradually from $i_{L(min)}$ to $i_{L(max)}$ at a rate of

$$\frac{di_L}{dt} = m = \frac{V_{dc} - V_{bat}}{L} = \frac{V_{L(max)}}{L}, \tag{3.22}$$

The rms value of the current through Q_1 is calculated as [31]

$$\begin{aligned} I^2_{Q1(rms)} &= \frac{1}{T_s} \int_0^{T_s} i^2_{Q1} dt \\ &= \frac{1}{T_s} \int_0^{D_1 T_s} \left(i_{L(min)} + mt \right)^2 dt \\ &= \frac{1}{T_s} \left[\frac{1}{3m} \left(i_{L(min)} + mt \right)^3 \right]_0^{D_1 T_s} \\ &= \frac{1}{3mT_s} \left[\left(i_{L(min)} + mD_1 T_s \right)^3 - i^3_{L(min)} \right] \\ &= 68.9 \text{ A}^2, \end{aligned} \tag{3.23}$$

where D_1 was calculated in (3.3). The total losses for Q_1 are thus

$$\begin{aligned} P_{Q1} &= P_{switch} + P_{cond} = P_{switch} + R_{DS(on)} I^2_{Q1(rms)} \\ &= 6.66 \text{ W} + 5.16 \text{ W} = 11.82 \text{ W}. \end{aligned} \tag{3.24}$$

The power loss due to the forward voltage of the MOSFET's freewheeling diode is

$$P_D = V_{SD} I_d, \tag{3.25}$$

where I_d is the mean current flowing through the diode over one switching period. The graph in the IRFP264 MOSFET datasheet shows a forward diode voltage (V_{SD}) of approximately 0.8 V at 10 A of current. The mean diode current of Q_2 is calculated as

$$I_{d2} = I_L D_2 = (10)(0.3143) = 3.143 \text{ A}. \tag{3.26}$$

Thus, the diode conduction power loss in Q_2 is

$$P_{D2} = V_{SD} I_{d2} = (0.8)(3.143) = 2.51 \text{ W}. \tag{3.27}$$

The total power losses for the top-half of the converter circuit whilst charging the batteries are

$$P_T = P_{Q_1} + P_{D_2} = 14.33 \text{ W}. \tag{3.28}$$

The total power losses of the bottom-half circuit are however also equal to P_T since the losses in Q_4 are equal to that of Q_1 and similarly the losses of Q_3 are equal to that of Q_2 due to the identical circuit operation described earlier. The top- and bottom-half of the converter circuit will be manufactured on separate printed circuit boards, each with their own heat sink. The power losses for the two sections are thus not added together.

CASE 2: Negative Inductor Current

For the case where current will flow in order to charge the dc bus, the switches will operate differently. Current will now flow through the diode of Q_1 (causing diode conduction losses) and through the MOSFET of Q_2 (causing switching as well as conduction losses).

First consider the losses in Q_2. The switching losses in Q_2 are identical to the switching losses calculated for Q_1 in (3.20) in the previous case (see current waveforms in Fig. 3.3). The total switching losses for Q_2 are thus also 6.66 W.

The MOSFET conduction losses will differ from the previous case since the duty cycle of Q_2 is different to that of Q_1. Equation 3.22 describing the rate of change of the inductor current through Q_2 is written as

$$\frac{di_L}{dt} = m = \frac{-V_{bat}}{L} = \frac{V_{L(min)}}{L}. \tag{3.29}$$

The rms current through Q_2 is thus

$$\begin{aligned} I_{Q2(rms)}^2 &= \frac{1}{T_s}\int_0^{T_s} i_{Q2}^2 dt \\ &= \frac{1}{T_s}\int_0^{D_2T_s} \left(i_{L(min)} + mt\right)^2 dt \\ &= \frac{1}{3mT_s}\left[\left(i_{L(min)} + mD_2T_s\right)^3 - i_{L(min)}^3\right] \\ &= 31.56 \text{ A}^2, \end{aligned} \tag{3.30}$$

where $i_{L(min)}$ is -8.875 A and D_2 is 0.3143. From (3.21) and (3.30) the conduction loss for Q_2 is calculated as 2.37 W resulting in a total power loss of 9.03 W for Q_2.

From (3.26) the mean current I_{d2} through the diode of Q_1 is 6.857 A at an absolute mean inductor current of 10 A and duty cycle D_1. Substituting the value for I_{d2} into (3.25), the diode conduction loss for Q_1 is calculated as 5.49 W. The total power losses for the top-half of the converter circuit whilst charging the dc bus are

$$P_T = P_{D_1} + P_{Q_2} = 14.52 \text{ W}. \tag{3.31}$$

The total power losses for the bottom-half of the converter circuit will be the same as for the top-half.

From the two cases the most power is dissipated when current is flowing from the batteries into the dc bus. The power losses from the operation of the switches are converted into heat and thus an adequate heat sink is required. The heat sink is designed for the worst case scenario, thus the maximum total power of the two cases are used in the heat sink design which is 14.52 W. The rise in junction temperature due to the power dissipated in the MOSFETs and diodes are given by [11]

$$\Delta T_j = P_T \left(R_{\theta jc} + R_{\theta cs} + R_{\theta sa}\right), \tag{3.32}$$

where $R_{\theta jc}$, $R_{\theta cs}$ and $R_{\theta sa}$ are the junction-to-case, case-to-sink and sink-to-ambient thermal resistances of the MOSFETs. The assumed maximum rise in junction temperature is 50°C. From the datasheet $R_{\theta jc}$ and $R_{\theta cs}$ are given as 0.45°C/W and 0.24°C/W respectively. The sink-to-ambient thermal resistance is calculated as 2.75°C/W from (3.32). The size of the aluminium heat sink available is 190 mm × 150 mm with a base thickness of 5 mm which gives a sink-to-ambient thermal resistance of 0.37°C/W [32], which is more than adequate.

3.1.4 Soft-start Circuit

A two-stage soft-start circuit comprising pre- and post-charge mechanisms [33] are used to increase the dc bus voltage gradually to the desired 350 V rail-to-rail

voltage.

First consider the top-half of the converter circuit of Fig. 3.1 used to generate the +175 V bus voltage. Initially the dc bus voltage is at ground potential. Without any soft-start mechanism in place, as soon as the circuit is switched on, in-rush currents will charge the dc bus to the equivalent battery voltage through the MOSFET's freewheeling diodes. The pre-charge circuit shown in Fig. 3.5 is used to limit the battery in-rush current to 5 A by means of four parallel-connected 100 Ω resistors which are placed in series with the converter's battery. At such time as the bus capacitor C is charged to the equivalent battery potential (≈120 V), the resistors are short-circuited by a relay to effectively remove the resistors from circuit. Table 3.4 show the values of the components used in the pre-charge circuit.

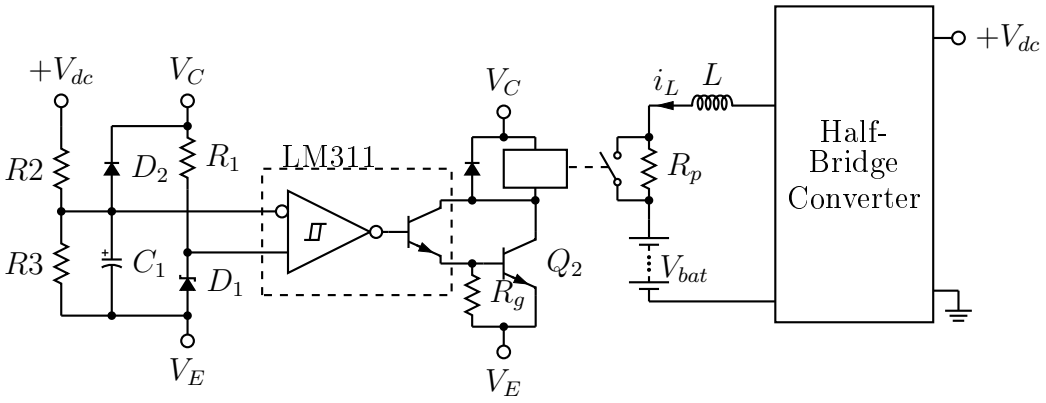

Figure 3.5: Pre-charge soft-start circuit implementation.

Table 3.4: Pre-charge soft-start circuit component values.

Component	Description	Value
V_C	-	12 V
V_E	-	0 V
R_p	-	25 Ω
Q_b	2N2219A NPN BJT	$I_c = 0.8$ A
R_g	-	10 kΩ
D_1	Zener diode	5.6 V
D_2	1N4148 switching diode	$V_F = 0.72$ V
C_1	-	10 μF
R_1	-	1 kΩ
R_2	-	220 kΩ
R_3	-	12 kΩ

The relay action is controlled by an LM311 comparator. A 5.6 V Zener diode is used as the reference voltage at the non-inverting input of the comparator, as shown in Fig. 3.5. A resistor divider circuit (R_2 and R_3) is used to scale down the dc bus voltage to the inverting input of the comparator. Once the scaled dc bus voltage exceeds the reference voltage, the inverting output of the comparator will change to a high state. This allows current to flow through the LM311's output transistor, thus closing the relay switch to create a short-circuit across the four parallel connected power resistors represented by R_p. Capacitor C_1 was added to introduce a small time delay in order to avoid any false state changes at the comparator's output during start-up. With the given resistor values the relay will trip at a measured dc bus voltage of

$$V_{dct} = \left(\frac{R_2 + R_3}{R_3}\right) V_{ref} = 108.3 \text{ V}, \tag{3.33}$$

which is low enough to avoid the relay from tripping while the converter is supplying power to a load, since the load can cause the battery voltage to drop slightly.

As seen in Fig. 3.5 the pre-charge circuit is connected in series between the converter's batteries and inductor. The rest of the converter circuit remains unchanged and is shown in Fig. 3.5 as a block diagram. The pre-charge circuit receives power from one of the ten 12 V batteries. To accommodate the required current to turn the relay switch on and off properly, an additional NPN BJT was added. Together with the LM311's output BJT they form a Darlington pair [34] where R_g is used to drain the capacitance.

A similar pre-charge circuit is used for the bottom-half of the converter circuit to gradually charge the dc bus to -120 V. The only difference is the scaled negative dc bus voltage feeds into the non-inverting input of the comparator and a negative 5.6 V reference voltage is used at the inverting input. The complete circuit schematic is shown in Appendix A.1.1.

The next stage of the soft-start circuit is used to charge the dc bus from the equivalent battery potential to the respective +175 V and -175 V rails. The post-charge mechanism is designed to limit current spikes once the switches start switching. To achieve this, the on-times of the switches have to gradually increase thus allowing the post-charge mechanism to control the duty-cycle of the switches by adjusting the dead-time.

At the instant Q_1 is switched off, there is a small but finite time delay before switch Q_2 is switched on, namely the dead-time. During this time period both switches remain off. The practical implementation of dead-time for switches Q_1 and Q_2 are demonstrated in Fig. 3.6. The modulator reference signal v_e (which is generated by the control circuit) is indicated in black and the triangular carrier waveform v_c is indicated in green in Fig. 3.6. If no dead-time were implemented, both switches will have a duty cycle of 50 %. An offset voltage V_{offs} is subtracted from v_e to generate the modulator reference

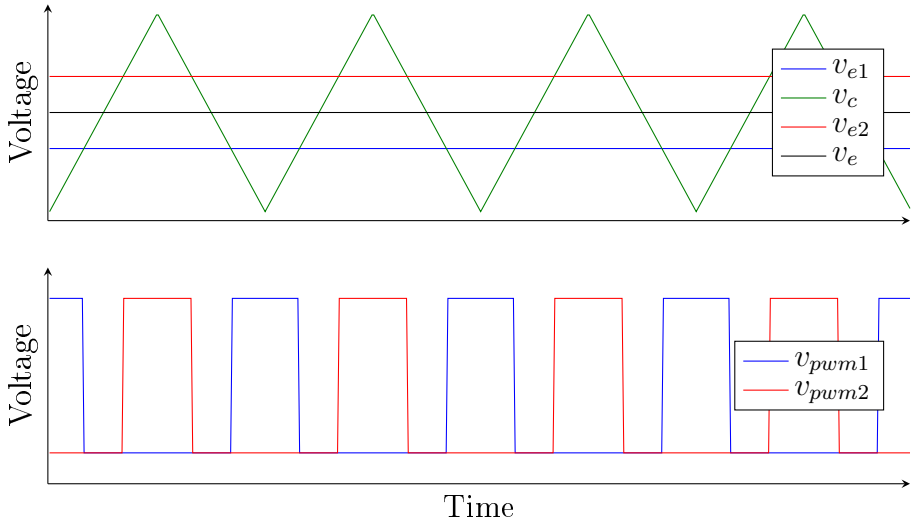

Figure 3.6: Dead-time implementation.

voltage v_{e1} for switch Q_1 and similarly V_{offs} is added to v_e to generate the modulator reference voltage v_{e2} for Q_2.

The on-time of the switches are determined as follows: if v_{e1} is greater than v_c, Q_1 is on and if v_{e2} is less than v_c, Q_2 is on. The resulting PWM signals for Q_1 and Q_2 are shown in the bottom graph of Fig. 3.6. The implemented dead-time is seen to have reduced the duty cycles of both switches. The dead-time is adjusted by changing the magnitude of the offset voltage V_{offs}.

The post-charge circuit functions by initially setting V_{offs} to a value larger than the magnitude of the carrier waveform, thus both switches will have a duty cycle of zero. After the dc bus has reached the equivalent battery potential, the offset voltage is progressively ramped down over a period of approximately 10 s to a minimum value, thus limiting the on-time and duty cycles of both switches, but allowing them to start switching.

The ramping down of the offset voltage is controlled by a capacitor and resistor circuit as shown in Fig. 3.7 with the component values given in Table 3.5.

Table 3.5: Post-charge soft-start circuit component values.

Component	Value
V_{Ref}	5 V
C_2	470 μF
D_3	$V_F = 0.72$ V
R_4	170 kΩ
R_5	1.8 kΩ
R_6	5.6 kΩ

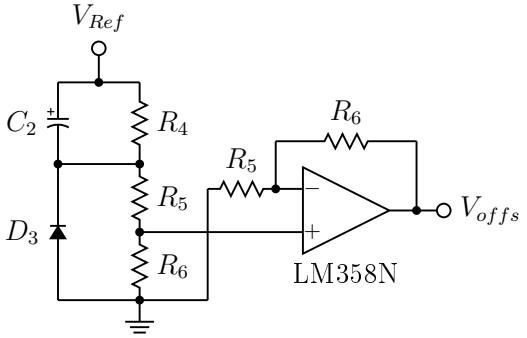

Figure 3.7: Post-charge soft-start circuit implementation.

As the voltage across C_2 increases when charged through R_5 and R_6, V_{offs} decreases until the minimum value of 0.44 V is reached. The minimum value corresponds to a dead-time of 1 μs and was chosen as such to eliminate any MOSFET shoot-through currents. Resistor R_4 is adjustable to increase or decrease the dead-time.

3.1.5 Isolated Gate-Drive Circuitry

An isolated gate-drive circuit is employed to communicate the switching signals generated by the converter's control circuit to the gate of each MOSFET. Galvanic isolation between the switches and the control circuit is essential to prevent damage to the control circuit due to the large voltage excursions encountered by the MOSFETs.

Each isolated gate-drive circuit comprises an optocoupler [11], a simple push-pull oscillator circuit (oscillating at approximately 300 kHz), a small toroidal transformer (with split primary and secondary windings), and two fast rectifier diodes. The oscillator supplies power to the optocoupler via the transformer and fast rectifier diodes as shown in Fig. 3.8, with the corresponding component values given in Table 3.6, while the optocoupler communicates the switching signals to the gate of a MOSFET.

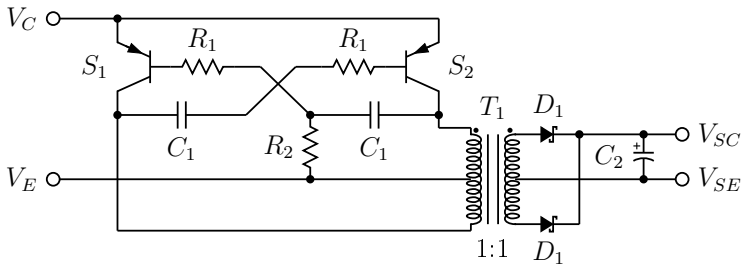

Figure 3.8: Power section of the isolated gate-drive circuit.

Table 3.6: Component values used in oscillator gate-drive circuit.

Component	Description	Value
V_C	Battery supply voltage	12 V
V_E	Battery supply voltage	0 V
S_1	PNP BC556 BJT	I_c = 100 mA
R_1	-	220 Ω
C_1	-	100 pF
R_2	-	1 MΩ
D_1	BAT85 Schottky diode	I_F = 200 mA
C_2	-	100 μF
V_{SC}	Isolated supply voltage	12 V
V_{SE}	Isolated supply voltage	0 V

An EPOS B64290 toroid was wounded with 10 turns of thin enamel copper wire on both sides to construct the transformer T_1 with a turns ratio of one-to-one. The TLP250 was used for the optocoupler as it is equipped with under-voltage lockout protection. The characteristics of the TLP250 is given in Table 3.7.

Table 3.7: TLP250 characteristic values.

Parameter	Description	Value
V_{CC}	Supply voltage	10-35 V
I_O	Output current	±1.5 A
V_{iso}	Isolation voltage	2500 V
t_p	Propagation delay time	150 ns
CM	Common mode transient immunity	5000 V/ μs

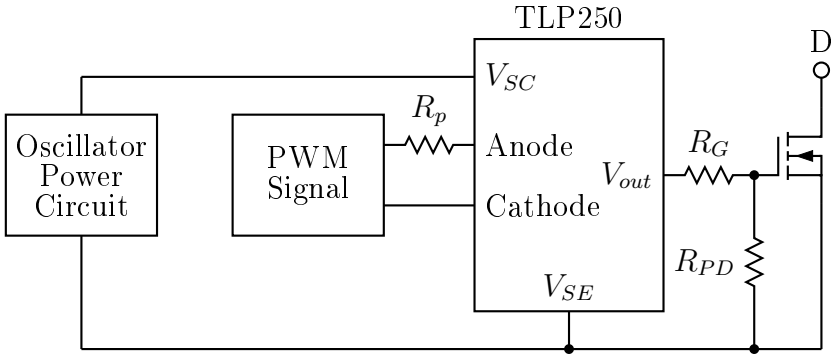

Figure 3.9: Block diagram of the MOSFET gate-drive circuit.

Four gate-drive circuits as shown in the block diagram of Fig. 3.9 are required, one for each MOSFET. The value of the resistor R_p was chosen as 220 Ω to limit the input current to the TLP250 to approximately 15 mA. A pull-down resistor R_{PD} of 4.7 kΩ is used to drain the gate capacitance once the MOSFET switches off. The gate resistor was chosen as 27 Ω. The maximum output voltage of the optocoupler with the described power circuit is 12 V, hence the maximum current the optocoupler is ever required to source is

$$I_O = \frac{V_{out}}{R_g} = \frac{12}{27} = 0.44 \text{ A}. \tag{3.34}$$

The datasheet of the TLP250 optocoupler specifies a maximum output current of 1.5 A. The optocoupler will thus be able to source the above mentioned current to the gate of the MOSFET.

The maximum voltage across any of the MOSFETs is the dc bus voltage of 175 V. With the turn-off time given as 92 ns in the MOSFET datasheet and the turn-on time as 99 ns, the minimum transient immunity required by the optocoupler is 1902 V/μs. The 5000 V/μs rated transient immunity of the optocoupler is thus sufficient.

A detailed schematic showing the isolated gate drivers, pre-charge soft-start circuit and complete converter circuit for both positive and negative dc bus generation can be found in Appendix A.1.1.

3.2 PWM Controller Design

A block diagram of the two identical controllers (one for each half-bridge converter) is shown in Fig. 3.10. Two control loops are used; an inner current control loop which is enclosed by an outer voltage control loop. The controller is structured such that the inner control loop measures and compares the mean inductor current I_L to a set-point voltage v_{seti} generated by the outer control loop. The set-point voltage corresponds to a current reference where 1 V represents 2 A of current. The output of the voltage controller v_{refi} is limited to v_{seti} as shown in Fig. 3.10 to effectively limit the average inductor current. The outer control loop measures and compares the dc bus voltage v_{dc} to a fixed set-point V_{dc}^* corresponding to a bus voltage of positive or negative 175 V respectively.

The current control loop is responsible for generating the PWM signals that feed the gates of the MOSFETs on the converter circuit. The output of the current controller produces an modulator reference signal v_e that is used for comparison with the carrier waveform to generate the required PWM signals. The reference signal is limited as seen in Fig. 3.10 to ensure the amplitude of the reference signal never exceeds the amplitude of the carrier waveform. It thus limits the duty cycle of the switches to a value below 100 %. The PWM

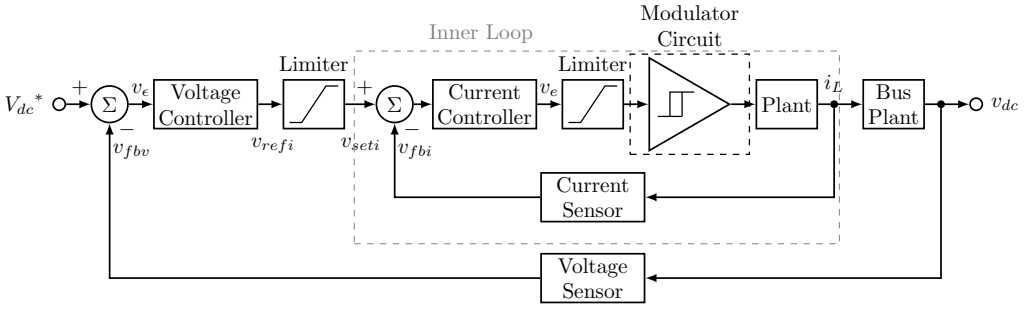

Figure 3.10: Block diagram of converter's control circuit.

generation circuit is denoted in Fig. 3.10 as the modulator circuit and will be described in more detail in the subsections that follow.

Frequency domain analysis is employed to design the voltage and current controllers. However, a time domain analysis of the circuit is also required to linearise the system and to provide the necessary differential equations to implement a time domain simulation of the converter and controller in the next chapter.

3.2.1 Carrier Waveform Generation

A 40 kHz triangular waveform is chosen as the carrier waveform to generate the required PWM signals. A 4 MHz crystal-controlled square-wave oscillator is scaled down to 40 kHz using two Hex D-type flip-flops, five flip-flops from each in order to divide by 100. The resulting square-wave is integrated to generate a triangular waveform. The dc component is removed (to prevent the integration of a constant) by capacitively coupling the output of the integrator circuit to the gain-stage op-amp (an LF353), which is also used to buffer the output waveform. The circuit outline is shown in Fig. 3.11 and the component values are given in Table 3.8. The triangular waveform at the output has a peak-to-peak value of 11 V.

The integrator is in actual fact a low-pass filter with a low corner frequency of

$$f_c = \frac{1}{2\pi R_3 C_2} = 159.2 \text{ Hz}, \tag{3.35}$$

to limit the dc gain while still functioning as an integrator at 40 kHz. The problem with using a pure integrator (by removing R_3) is without any dc feedback, the output voltage will tend to drift until the op-amp saturates due to the op-amp's internal offset and bias currents. By adding R_3, dc feedback is provided and the output voltage is stabilised [35].

The not-gates used are provided by a 74HC14 hex inverting Schmitt trigger integrated circuit (IC) package containing 6 inverting buffers. Both the

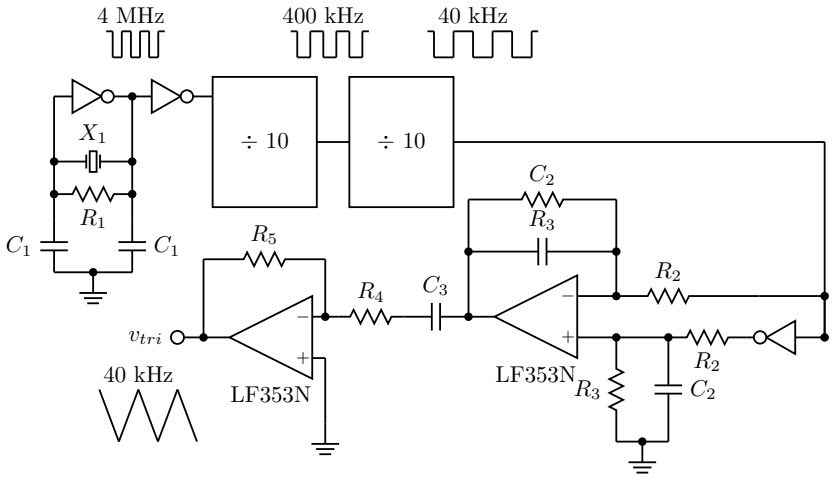

Figure 3.11: Circuit outline of the triangular carrier waveform generation.

Table 3.8: Triangular waveform generator component values.

Component	Value
X_1	4 MHz
R_1	10 MΩ
C_1	22 pF
R_2	22 kΩ
R_3	1 MΩ
C_2	1 nF
C_3	100 nF
R_4	1.2 kΩ
R_5	4.7 kΩ

74HC14 and 74HC174 IC packages require a supply voltage of 5 V.

3.2.2 Controller Plant

For the analysis and design of the controller only the top-half of the converter circuit is used as shown in Fig. 3.12. The same control circuit is implemented in the bottom-half of the converter. The plant portion of the converter includes the current sense resistors used by the current control loop to generate the current feedback measurement and is denoted by R_{cs} in Fig. 3.12.

With reference to Fig. 3.12 the equation describing the inductor current as a function of the mid-point voltage v_m is given by

$$v_m - V_{bat} - i_L\left(R_{in} + R_{cs}\right) = L\frac{di_L}{dt}. \tag{3.36}$$

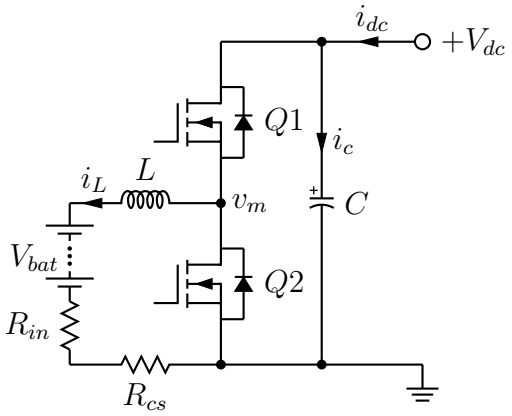

Figure 3.12: Bidirectional dc-dc converter circuit used for controller design.

The differential equation for the inductor current is thus

$$\frac{di_L}{dt} = \frac{v_m - V_{bat} - i_L\left(R_{in} + R_{cs}\right)}{L}, \tag{3.37}$$

where

$$v_m = s_1 v_{dc}. \tag{3.38}$$

The variable s_1 dictates the state of switch Q_1 where $s_1 = 1$ indicates the switch is on and $s_1 = 0$ indicates Q_1 is off. The mid-point voltage is thus at either $+V_{dc}$ or zero depending on the amplitude of the modulator reference voltage with respect to the carrier waveform. If the reference voltage v_e at time t is larger than the carrier waveform v_{tri}, $s_1 = 1$, otherwise $s_1 = 0$.

For frequency domain analysis the effect of the battery voltage is omitted since it is considered a constant dc value. Hence, the mean voltage V_m measured at the mid-point between switches Q_1 and Q_2 is given by

$$V_m = (sL + R_{in} + R_{cs})I_L, \tag{3.39}$$

where I_L is the mean battery and inductor current. Solving (3.39) the forward transfer function of the controller plant $G_p(s)$, describing the mean inductor current as a function of the mid-point voltage, is given by

$$G_p(s) = \frac{I_L}{V_m} = \frac{1}{sL + R_{in} + R_{cs}}. \tag{3.40}$$

3.2.3 Current Control Loop

The current control loop, shown in Fig. 3.13, functions to regulate the mean inductor current flowing to and from the batteries by controlling the switching actions of the MOSFETs. The time-varying modulator reference voltage v_e is

compared (by means of a high-speed AD790JN comparator from Analog Devices) to the triangular waveform described in Section 3.2.1, where the output of the comparator provides the PWM switching signal.

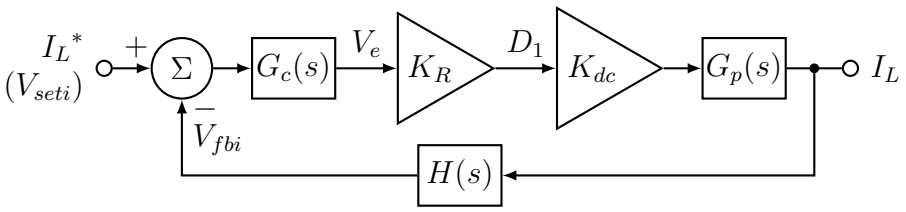

Figure 3.13: Current control loop block diagram.

A linear model of the modulator circuit is assumed, where the duty cycle of the PWM signal D is calculated as the ratio of the mean modulator reference voltage V_e to the amplitude of the carrier waveform. Assuming the triangular carrier waveform has a minimum value of 0 V and a maximum value of V_R, the duty cycle D is:

$$D = \frac{V_e}{V_R}. \tag{3.41}$$

To account for the linear PWM model constant K_R is introduced in Fig. 3.13. From (3.41) the constant K_R is expressed as the ratio of the duty cycle to the modulator reference voltage, thus

$$K_R = \frac{D_1}{V_e} = \frac{1}{V_R}, \tag{3.42}$$

where D_1 is the duty cycle of switch Q_1. With reference to Fig. 3.12 the mean mid-point voltage V_m is related to the duty cycle (as proven in Section 2.2.2) by

$$V_m = D_1 V_{dc} = \frac{V_e}{V_R} V_{dc}. \tag{3.43}$$

For the design of the current controller the dc bus voltage is assumed constant, which is reasonable given that the current control loop is specifically designed to respond significantly faster than the voltage control loop. Constant K_{dc} is thus 175 V. From (3.43) the mid-point voltage is the duty cycle multiplied by K_{dc}.

Ten parallel connected 0.68 Ω metal film resistors were used for current sensing. The feedback voltage V_{fbi} provided to the inverting input of the summation in Fig. 3.13, is thus the product of the inductor current I_L and the feedback transfer function $H(s)$. The current-sensing feedback circuit is shown in Fig. 3.14 with the corresponding component values given in Table 3.9.

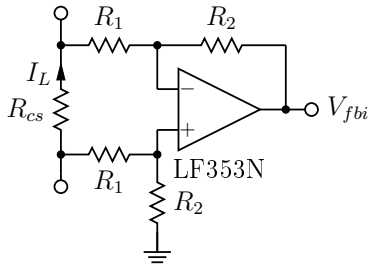

Figure 3.14: Inductor current sensing circuit.

Table 3.9: Component values for the current sense circuit.

Component	Value
R_{cs}	68 mΩ
R_1	4.7 kΩ
R_2	34.5 kΩ

A differential signal from the current sense resistors feed an LF353N op-amp through resistors to add the required gain. The transfer function $H(s)$ is thus given by

$$H(s) = \frac{V_{fbi}}{I_L} = \frac{R_2}{R_1} R_{cs}. \tag{3.44}$$

A gain of 7.34 ($\frac{R_2}{R_1}$) is used such that at a maximum current of 10 A the feedback signal will be 5 V. Similarly in the time domain the current loop feedback voltage is given by

$$v_{fbi} = \frac{R_2}{R_1} R_{cs} i_L. \tag{3.45}$$

With reference to Fig. 3.13, the open-loop transfer function is

$$G_{ol}(s) = G_c(s) K_R K_{dc} G_p(s) H(s), \tag{3.46}$$

where $G_c(s)$ is the compensation amplifier. The frequency domain analysis of $G_{ol}(s)$ without the transfer function of the compensation amplifier present is shown in Fig. 3.15. In adherence with the Nyquist stability criterion, the open-loop transfer function with compensation is required to have both positive phase and gain margins in order for the closed-loop transfer function to be stable (not oscillate). The phase margin should, preferably, be at least 30° [36]. Furthermore, the unity gain crossover frequency of the open-loop transfer function should be chosen according to the desired performance of the system, but is generally designed to be at around one-fifth of the system's switching frequency or lower [37].

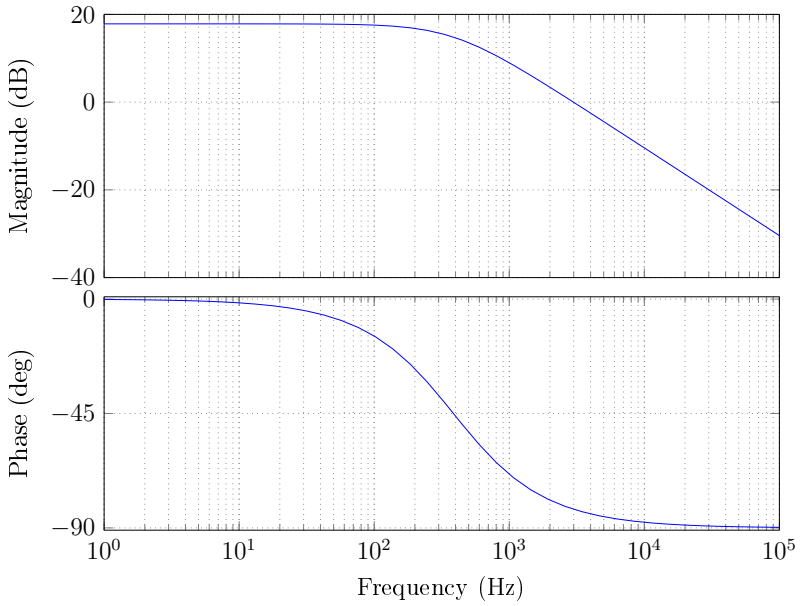

Figure 3.15: Bode plot of current controller without compensation.

As seen from Fig. 3.15 the phase margin is positive, the unity crossover frequency is at 2.99 kHz and the dc gain is 17.8 dB. The corner frequency is at 390 Hz. A compensation amplifier will increase the bandwidth as well as the dc gain. Ideally the dc gain should strive to infinity thus an additional pole is required.

In order to improve the bandwidth as well as the dc gain a PI or pole-zero compensator [38] is required. As the name suggests, the last mentioned consists of a pole-zero pair, where the pole and zero are placed to achieve the required closed-loop stability of the system. The pole-zero and PI compensators are very similar, the only benefit of using a pole-zero compensator is the additional pole present at high frequencies. This allows a roll-off of -40 dB per decade below the 0 dB which helps to improve the filtering of switching noise. A pole-zero compensation amplifier as shown in Fig. 3.16 is chosen as the compensator $G_c(s)$ for the current control loop due to the good transient response and load regulation that it provides.

The differential equations describing the pole-zero compensator are derived by assuming the amplifier is an inverting amplifier with the non-inverting input grounded. The inverting input voltage is defined as $v_{fbi} - v_{seti}$. From first principles it is known that the currents flowing into the amplifier inputs sum to zero, thus

$$\frac{v_{fbi} - v_{seti}}{R_1} + C_1 \frac{dv_e}{dt} + C_2 \frac{dv_{c2}}{dt} = 0, \tag{3.47}$$

where the voltage across capacitor C_1 is the reference voltage v_e. The voltage

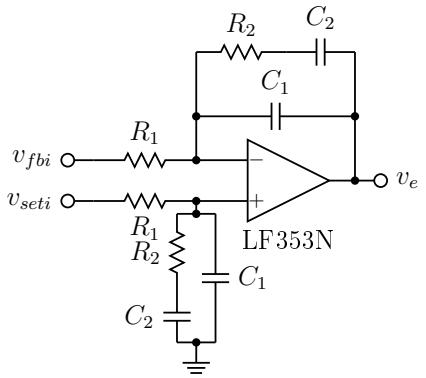

Figure 3.16: Pole-zero compensation amplifier.

across C_2 is defined as v_{c2} and can also be expressed by

$$v_{c2} = v_e - i_{c2}R_2 = v_e - C_2R_2\frac{dv_{c2}}{dt}. \tag{3.48}$$

Solving the above differential equation yields

$$\frac{dv_{c2}}{dt} = \frac{v_e - v_{c2}}{C_2R_2}. \tag{3.49}$$

Substituting (3.49) into (3.47) and rearranging results in the differential equation for the modulator reference voltage v_e where

$$\frac{dv_e}{dt} = \frac{v_{seti} - v_{fbi}}{C_1R_1} + \frac{v_{c2} - v_e}{R_1R_2}. \tag{3.50}$$

Similarly for the frequency domain analysis the transfer function $G_c(s)$ is derived below. Firstly,

$$\begin{aligned} Z_f &= \left(R_2 + \frac{1}{sC_2}\right) || \frac{1}{sC_1} \\ &= \left(\frac{sC_2R_2 + 1}{sC_2}\right) || \frac{1}{sC_1} \\ &= \frac{1}{\frac{sC_2}{sC_2R_2+1} + sC_1} \\ &= \frac{sC_2R_2 + 1}{s^2C_1C_2R_2 + s(C_1 + C_2)}, \end{aligned} \tag{3.51}$$

where Z_f is the combined amplifier feedback impedance. The transfer function for Fig. 3.16 is thus

$$\begin{aligned} G_c(s) &= \frac{V_e}{V_{seti} - V_{fbi}} \\ &= \frac{Z_f}{R_1} \\ &= \frac{sC_2R_2 + 1}{R_1\left[s^2C_1C_2R_2 + s(C_1 + C_2)\right]}, \end{aligned} \tag{3.52}$$

and in standard form

$$\begin{aligned} G_c(s) &= \frac{\frac{sC_2R_2+1}{C_1+C_2}}{sR_1\left(\frac{sC_1C_2R_2}{C_1+C_2} + 1\right)} \\ &= \frac{1}{R_1(C_1 + C_2)}\left[\frac{sC_2R_2 + 1}{s\left(\frac{sC_1C_2R_2}{C_1+C_2} + 1\right)}\right]. \end{aligned} \tag{3.53}$$

The dc gain in decibels is

$$G_{cgain} = 20\log_{10}\left[\frac{1}{sR_1(C_1 + C_2)}\right]. \tag{3.54}$$

The two time constants are

$$\tau_1 = C_2R_2, \tag{3.55}$$

and

$$\tau_2 = \frac{C_1C_2R_2}{C_1 + C_2}, \tag{3.56}$$

with corresponding corner frequencies of

$$f_1 = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi}\left(\frac{1}{C_2R_2}\right), \tag{3.57}$$

and

$$f_2 = \frac{1}{2\pi\tau_2} = \frac{1}{2\pi}\left(\frac{C_1 + C_2}{C_1C_2R_2}\right). \tag{3.58}$$

As seen from (3.53), the pole-zero compensator has an integrator pole which will give the required infinite dc gain. The first corner frequency f_1 should be less than or equal to the corner frequency of the open-loop response (390 Hz) shown in Fig. 3.15 in order to increase the bandwidth. The inductor current ripple will impose a ripple voltage on the reference signal V_e. To ensure the ripple on the reference voltage is filtered out properly (to produce a constant reference voltage), the desired bandwidth for the current controller is at around

one tenth of the switching frequency, thus at 4 kHz. The second corner frequency should be below the 0 dB line thus at a value equal to or higher than 4 kHz. Substituting (3.57) into (3.58) gives

$$f_2 = \left(\frac{C_1 + C_2}{C_1}\right), \tag{3.59}$$

where the desired corner frequency for f_1 is chosen as 100 Hz and for f_2 as 5 kHz, resulting in a relationship between C_1 and C_2 of

$$C_2 = 49C_1. \tag{3.60}$$

The value chosen for C_1 is 10 nF and by taking the above equation into account, the closest value for C_2 is 470 nF. From (3.57) the calculated value of R_2 is 3.4 kΩ. The bandwidth of the controller will change from 2.99 kHz to 4 kHz by adjusting the gain factor G_{cgain}. Since the roll-off of the controller is at -20 dB/decade when it crosses the 0 dB line the amount of gain required to change the controller's bandwidth is calculated as

$$\Delta G_{cgain} = 20\log_{10}(4000) - 20\log_{10}(2990) = 2.53 \text{ dB}. \tag{3.61}$$

From (3.54) and (3.61) the value of R_1 is calculated as 3.99 kΩ. After testing and simulation some of the values had to be adjusted slightly. The final component values are given in Table 3.10.

Table 3.10: Component values for the current loop compensator.

Component	Value
R_1	3.3 kΩ
R_2	4.7 kΩ
C_1	10 nF
C_2	470 nF

The closed-loop transfer function of the complete current controller shown in Fig. 3.13 is

$$G_{cl}(s) = \frac{I_L}{V_{seti}} = \frac{G_c(s)K_R K_{dc} G_p(s)}{1 + G_c(s)K_R K_{dc} G_p(s)H(s)}. \tag{3.62}$$

To ensure the stability of the system with the compensation amplifier present, the open-loop response of the current controller is investigated. Fig. 3.17 shows the Bode plot of both the open- and closed-loop responses. The open-loop response shows a phase margin of 53.8 degrees and a unity gain crossover frequency of 3.2 kHz. The closed-loop response shows a dc gain of 6.04 dB corresponding to a static loop sensitivity of 2.0 A of battery current per volt of

excitation applied to the set-point input V_{seti}. Thus, at an absolute maximum set-point voltage of 5 V, the battery current will rise to 10 A as desired.

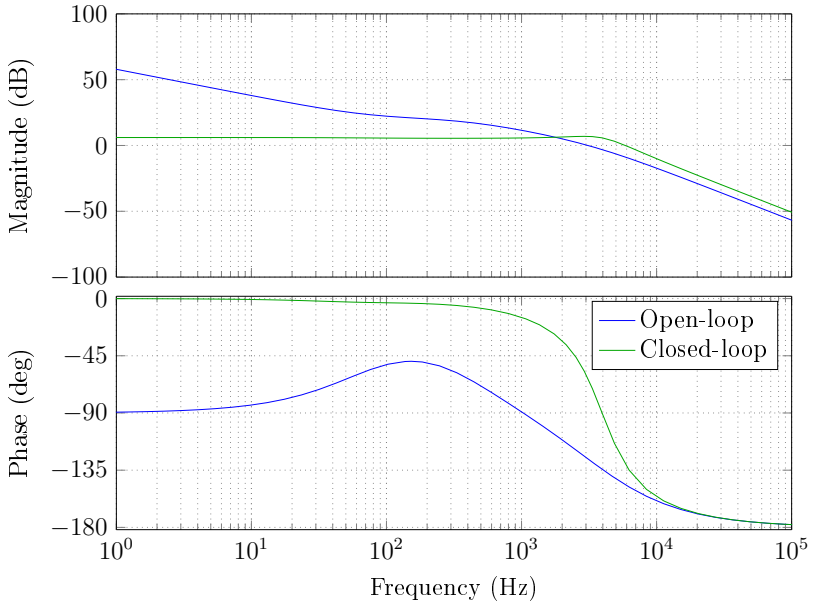

Figure 3.17: Current controller bode plot.

In Fig. 3.17 the gain margin is shown to be infinite as the phase plot of the open-loop response never crosses the -180 degree line. Since an infinite gain margin cannot be realised in practice, a bifurcation test [39] was undertaken to determine a more realistic prediction of the gain margin. A gain variable K_B was added to the compensation circuit as shown in Fig. 3.18 such that the transfer function for the compensation amplifier changed to $K_B G_c(s)$.

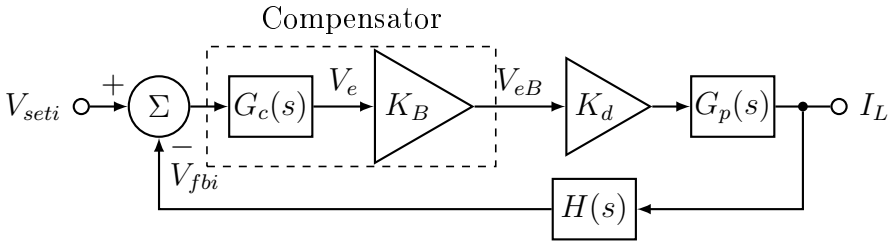

Figure 3.18: Current control loop with additional gain factor K_B.

The gain variable K_B was linearly increased from one to 40 in a MATLAB Simulink model of the converter circuit and controller. The result of the bifurcation test is shown in Fig. 3.19. An additional gain of 22 was added to the compensation circuit, where the output reference voltage V_{eB} feeds the PWM

comparator, before the output voltage V_e of the controller $G_c(s)$ was observed to bifurcate. This indicates a more realistic gain margin of 26.8 dB. A positive gain and phase margin suggest that the current control loop is stable.

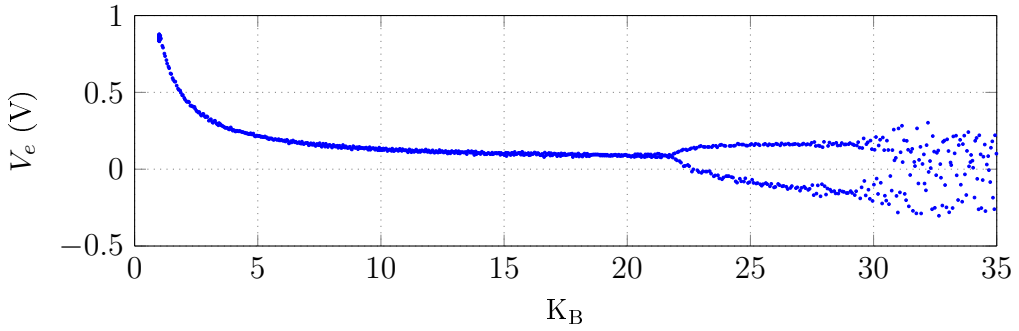

Figure 3.19: Bifurcation diagram used for stability analysis.

3.2.4 Current and Voltage Limiting Circuit

An active clamp circuit [35] shown as a limiter in Fig. 3.10 is used to limit the absolute maximum of the mean current demanded from the battery. This action is realised by clamping the range of the set-point current dictated by the voltage control loop to -10 A and +10 A. The clamp circuit in Fig. 3.20 shows both positive and negative voltage clamping where the reference voltages can be made adjustable.

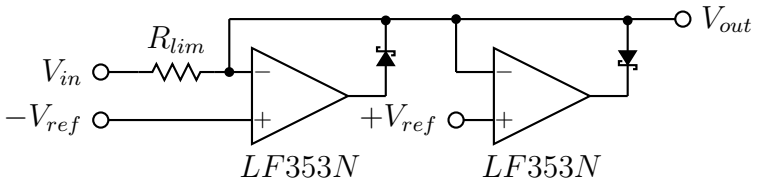

Figure 3.20: Postive and negative active clamping circuit.

Since the current control loop has a static loop sensitivity of 2 A per volt of excitation at the set-point input, the values for -V_{ref} and -V_{ref} are set to plus and minus 5 V respectively, to correspond to the current limit of -10 A to +10 A. The input voltage V_{in} is the reference set-point v_{refi} produced by the voltage control loop while the output voltage V_{out} is the limited set-point voltage v_{seti} for comparison with v_{fbi}. The resistor used for R_{lim} is 470 Ω and the two diodes are BAT85 Schottky diodes.

The same circuit was used to limit the output of the compensation amplifier $G_c(s)$ to -5 V and +5 V so as to clamp the range of the modulator reference

signal. With the triangular waveform at a 5.5 V amplitude (11 V peak to peak) and a maximum reference voltage of +5 V, the maximum duty cycle is limited to 95 %. Similarly the minimum duty cycle is limited to 5 % at a minimum reference signal of -5 V.

3.2.5 Voltage Control Loop

The voltage control loop functions to regulate the dc bus voltage v_{dc} to the corresponding voltage set-point $V_{dc}{}^{*}$. The bus plant portion of the controller block diagram shown in Fig. 3.10 contains dc bus capacitors of the converter circuit. The dc bus voltage is related to the rest of the converter circuit through the current flowing into the capacitors and the capacitors themselves. The current flowing into the capacitor as shown Fig. 3.12 is related to the inductor current by

$$i_c = i_{dc} - s_1 i_L, \tag{3.63}$$

where s_1 is again used to determine the state of switch Q_1 as either on ($s_1 = 1$) or off ($s_1 = 0$). The current through the capacitor is also defined as

$$i_c = C\frac{dv_c}{dt} = C\frac{dv_{dc}}{dt}. \tag{3.64}$$

Combining (3.63) and (3.64) results in the differential equation describing the dc bus voltage as a function of the inductor current and is given below as

$$\frac{dv_{dc}}{dt} = \frac{i_{dc} - s_1 i_L}{C}. \tag{3.65}$$

With $s_1 i_L$ averaged over at least 5 to 10 switching cycles, $\overline{s_1 i_L}$ is approximately equal to $d_1 i_L$, where d_1 is the instantaneous duty cycle of switch Q_1. Equation (3.65) time averaged over 5-10 switching cycles now becomes

$$\frac{dv_{dc}}{dt} = \frac{i_{dc} - d_1 i_L}{C}. \tag{3.66}$$

Both the inductor current i_L and the duty cycle d_1 are time-varying signals resulting in a non-linear differential equation for the dc bus voltage. For frequency domain analysis transfer functions are required to be linear. Thus (3.66) is linearised before applying the Laplace transform for frequency domain analysis. A function can be linearised around a certain operating point using a first order Taylor series approximation [40]. The approximation for (3.66) is thus

$$\begin{aligned} \dot{v}_{dc} = {} & f\left(d_1(0), i_L(0)\right) + \frac{\partial f}{\partial d_1}\Big|_{\substack{d_1=d_1(0)\\ i_L=i_L(0)}} \left(d_1(t) - d_1(0)\right) \\ & + \frac{\partial f}{\partial i_L}\Big|_{\substack{d_1=d_1(0)\\ i_L=i_L(0)}} \left(i_L(t) - i_L(0)\right), \end{aligned} \tag{3.67}$$

and in increment form

$$\frac{d\Delta v_{dc}(t)}{dt} = \frac{\partial f}{\partial d_1}\Big|_{\substack{d_1=d_1(0)\\ i_L=i_L(0)}} \Delta d_1(t) + \frac{\partial f}{\partial i_L}\Big|_{\substack{d_1=d_1(0)\\ i_L=i_L(0)}} \Delta i_L(t), \tag{3.68}$$

where f is the differential equation $\frac{dv_{dc}}{dt}$ given in (3.66). The operating point of the duty cycle d_1 is around 0.6857 and denoted as $d_1(0)$. The operating point for the inductor current $i_L(0)$ is calculated as

$$\frac{dv_{dc}}{dt} = 0 = \frac{i_{dc} - d_1(0)i_L(0)}{C}. \tag{3.69}$$

Rearranging the above equation:

$$i_L(0) = \frac{i_{dc}}{d_1(0)}. \tag{3.70}$$

The operating point for the inductor current thus depends on the amount of current flowing into the dc bus. Since this value will vary, the frequency and time domain analysis are conducted at the maximum and minimum mean dc bus current variation as well as at a mean dc bus current of zero. After evaluating (3.68) the linearised differential equation for the dc bus voltage is

$$\frac{d\Delta v_{dc}(t)}{dt} = -\frac{i_L(0)}{C}\Delta d_1(t) - \frac{d_1(0)}{C}\Delta i_L(t). \tag{3.71}$$

Multiplying both sides with C and taking the Laplace transform of the above equation, (3.71) becomes

$$-sCV_{dc}(s) = K_{d0}I_L(s) + K_{i0}D_1(s), \tag{3.72}$$

and after simplifying

$$V_{dc}(s) = \frac{K_{d0}I_L(s) + K_{i0}D_1(s)}{-sC} = F_p(s)\left[K_{d0}I_L(s) + K_{i0}D_1(s)\right], \tag{3.73}$$

where $F_p(s)$ is used to define the dc bus plant portion of the converter.
The block diagram of the linearised control system is shown in Fig. 3.21 where $F_c(s)$ denotes the controller for the voltage control loop. The feedback voltage V_{fbv} shown in Fig. 3.21 is a scaled version of the bus voltage, where K_s is the scaling factor. The block diagram in Fig. 3.21 can be manipulated by moving the branch point at $I_L(s)$ to $D_1(s)$ as shown in Fig. 3.22. By performing block diagram reduction the control system diagram reduces to the diagram shown in Fig. 3.23.

From Fig. 3.23 the open-loop transfer function of the voltage control loop is calculated as

$$F_{ol}(s) = \frac{K_s K_R F_c(s) G_c(s) F_p(s)}{1 + K_{dc}K_R G_c(s) G_p(s) H(s)}\left[K_{i0} + K_{dc}K_{d0}G_p(s)\right], \tag{3.74}$$

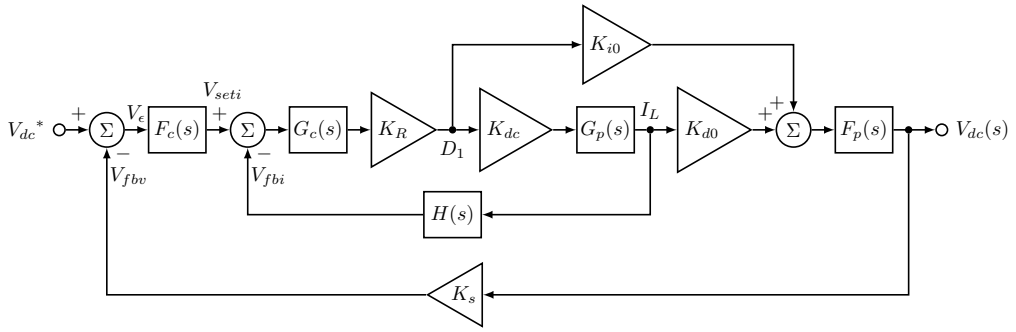

Figure 3.21: Voltage and current control loop block diagram.

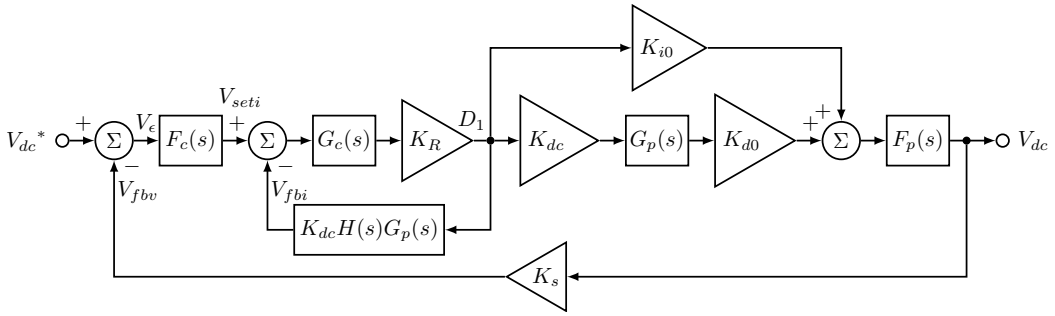

Figure 3.22: Simplified voltage and current control loop block diagram.

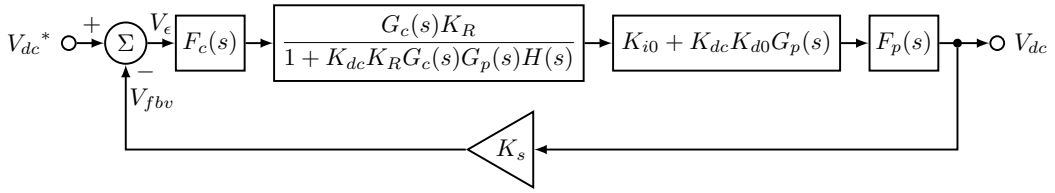

Figure 3.23: Reduced voltage and current control loop block diagram.

and the closed-loop transfer function as

$$F_{cl}(s) = \frac{V_{dc}(s)}{V_{dc}{}^*} = \frac{\frac{1}{K_s}F_{ol}(s)}{1+F_{ol}(s)}. \tag{3.75}$$

The measured dc bus voltage is scaled down through a differential amplifier functioning as an attenuator as shown in Fig. 3.24 with R_1 equal to 238 kΩ and R_2 equal to 6.5 kΩ. The equivalent scaling factor denoted K_2 in the voltage control loop is the ratio between R_2 and R_1 which is $\frac{1}{35}$. Thus at an ideal positive dc bus voltage of 175 V, the equivalent feedback voltage v_{fbv} is 5 V. The reference voltage $V_{dc}{}^*$ is therefore set to 5 V.

A 2 kW load is connected to the dc bus rails. The transfer function $F_p(s)$ given in (3.73), describing the dc bus plant portion of the system, is modelled

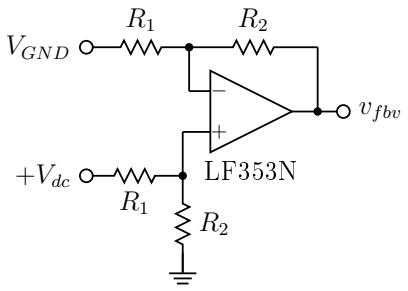

Figure 3.24: Bus voltage feedback circuit.

with and without the load present to confirm stability throughout. With the load R_{dc} connected the transfer function changes to

$$F_p(s) = \frac{-R_{dc}}{sCR_{dc} + 1}, \tag{3.76}$$

where the minimum value of the load is 60 Ω. The open-loop frequency response without the compensation amplifier $F_c(s)$ present is shown in Fig. 3.25 for the loaded as well as unloaded dc bus condition. The initial dc bus current is assumed zero, thus from (3.70) the operating point for the inductor current K_{i0} is also zero.

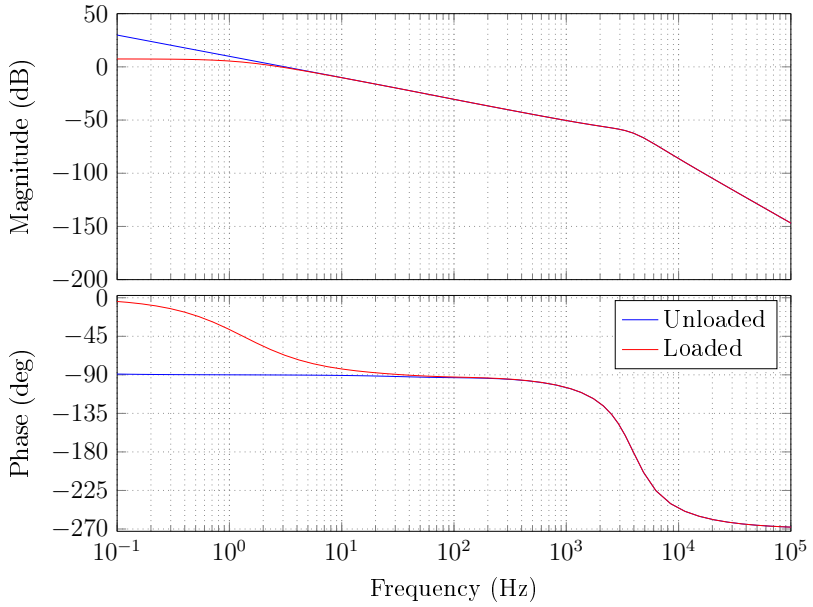

Figure 3.25: Bode plot of the voltage controller without compensation.

As seen from Fig. 3.25 when a 60 Ω load is connected the open-loop response does not have infinite gain at dc. A pole-zero compensator is once again chosen

as the compensation method since it will provide an additional pole to achieve an infinite dc gain and also provide the required additional bandwidth for the voltage control loop.

The difference between the set-point voltage $V_{dc}{}^*$ and the scaled bus voltage V_{fbv} is V_ϵ, which is the input to the voltage control loop's compensator, $F_c(s)$. The derivation for the two corner frequencies and dc gain component for a pole-zero compensator was shown in Section 3.2.3. The first corner frequency f_1 is chosen to be at 5 Hz which is where the bode plot shown in Fig. 3.25 rolls off at -20 dB/decade. The second corner frequency f_2 is chosen to be at a frequency of around 10 kHz which will be well below the 0 dB line once the dc gain is added. The bandwidth of the voltage controller should ideally be at around one tenth of the current control loop's, thus at 320 Hz.

The compensation amplifier is identical to the circuit shown in Fig. 3.16 where the two inputs are now V_{setv} and V_{fbv} and the output is V_{seti}. The same differential equations thus also apply. The component values were calculated in a similar manner to that of the current controller's compensation amplifier by using equations (3.54) through (3.59). The final component values are given in Table 3.11 with the corner frequencies at 33.8 Hz and 15.95 kHz respectively.

Table 3.11: Component values for the voltage loop compensator.

Component	Value
R_1	1 kΩ
R_2	100 kΩ
C_1	100 pF
C_2	47 nF

The bode plots for both the open- and closed-loop frequency responses of the voltage control loop are shown in Fig. 3.26 at a dc bus current of zero. A dc gain of 30.9 dB is indicated, corresponding to a static loop sensitivity of 35 V of bus voltage per volt of excitation applied to the set-point input. Thus, at a set-point value of 5 V, the bus voltage will rise to 175 V. A phase-margin, gain-margin and unity gain crossover frequency of 77.6 degrees, 20.8 dB and 294 Hz are further indicated, suggesting that the voltage control loop is stable under the specified conditions. Since a load connected to the dc bus only affects the controller at very low frequencies (below 50 Hz) the gain and phase margins remains the same under no-load conditions.

The stability of the voltage control loop was tested again at the mean minimum and maximum inductor current operating points of ±10 A. The open-loop frequency response results are summarised in Table 3.12.

The results show the voltage control loop will remain stable within the inductor current operating range with positive gain and phase margins for all

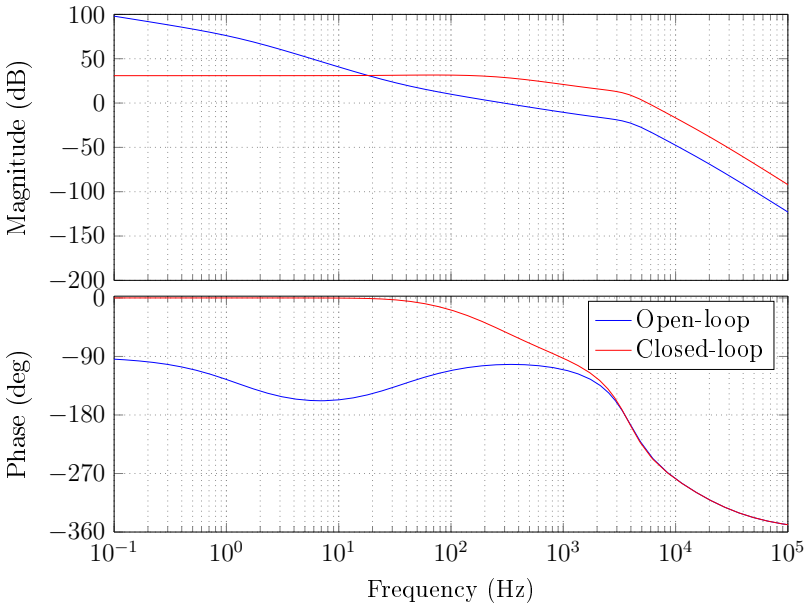

Figure 3.26: Bode plot of voltage controller under load.

Table 3.12: Stability analysis of the voltage control loop at various mean inductor current operating points.

K_{i0}	10 A	0 A	-10 A
Gain margin	24.2 dB	20.8 dB	17.1 dB
Phase margin	81.4°	77.6°	73.7°
Unity cross-over	319 Hz	294 Hz	270 Hz

conditions. A complete circuit schematics of the controllers used for both the top and bottom converter are shown in Appendix A.1.2.

3.3 Summary

The detailed design of the bidirectional dc-dc converter circuit was presented in this chapter. An overview of the basic circuit operation was given. The design of the dc-dc converter's double control loop control circuit was presented and the implementation thereof detailed. Both frequency and time domain equations were derived to describe the operation of the circuit. The frequency domain analysis showed both the inner and outer control loops are stable. The time domain analysis is presented in the next chapter along with the measured results from the manufactured prototype circuit for comparison purposes.

Chapter 4

DC-DC Converter Simulation and Test Results

In this chapter the operation of the designed dc-dc converter from the previous chapter is simulated in the time domain. This simulation is used to confirm the stability of the converter during start-up, as well as to examine the step response of the controller with both current and voltage control loops implemented. Various measurements are taken from the manufactured prototype circuit in order to validate the time domain simulations and to demonstrate the practical operation of the circuit.

Since the simulation of the negative bus voltage is identical to the inverted simulation of the positive bus voltage, only the top-half of the converter circuit (producing the positive bus voltage $+V_{dc}$) was used for simulation purposes. The simulations were implemented in MATLAB and corresponds to a simple iterative Euler solution of the relevant differential equations, (3.37), (3.38), (3.49), (3.50) and (3.65) from Chapter 3, that describe the behaviour of the circuit.

4.1 Test Set-Up

The dc-dc converter test set-up is shown in Fig. 4.1. The printed circuit boards (PCBs) used for the practical implementation of the converter are presented in Appendix B.1. The two power boards responsible for generating the positive and negative dc bus rails are mounted on two heat sinks as shown in Fig. 4.1. The control board is situated on top of the two heat sinks. A small 12 V fan is mounted on the side of the heat sinks to increase the airflow, thus cooling the heat sinks.

The batteries are located at the bottom of the trolley shown in Fig. 4.1. The two motors on-top of the batteries are used with the inverter circuit and are irrelevant to the measurements taken for this chapter. The circuit is switched on by the two circuit breakers at the front of the trolley where each circuit

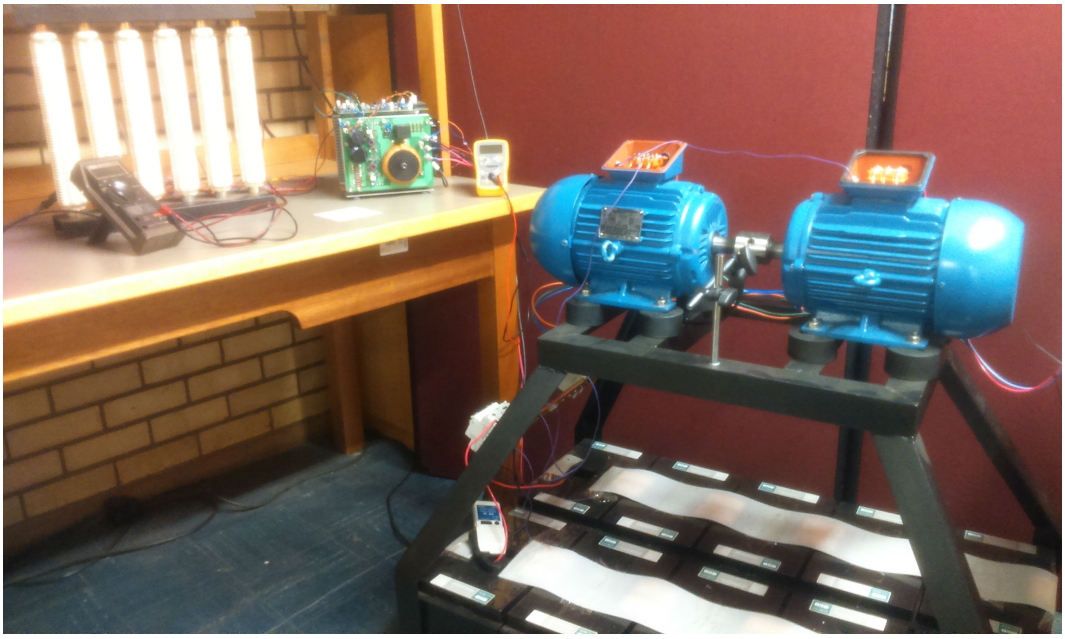

Figure 4.1: Converter prototype circuit test set-up.

breaker is connected to the positive and negative point of 10 series connected batteries.

The load used during testing is a 60 Ω resistive load comprising 6 series connected 10 Ω resistors to form a resistor bank. Each resistor is rated to handle 500 W and thus the six series connected resistors can handle a total power of 3 kW.

For safety purposes during measurements, the mid-point between the top- and bottom-half of the converter was used as the grounding point for all voltage probe connections.

4.2 Start-Up Response

The simulated dc-dc converter start-up response showing both the instantaneous dc bus voltage and inductor current are displayed in Fig. 4.2. This simulation includes the modelling of the soft-start circuit as well as the dead-time of the switches. A negative inductor current indicates current flowing from the batteries into the dc bus to charge the dc bus or power a load, while a positive inductor current indicates current flowing from the dc bus into the batteries thus charging the batteries.

As seen from Fig. 4.2 the first stage of the soft-start circuit, the pre-charge circuit, is active for the first 350 ms after start-up, during which time the bus voltage rises from zero to the equivalent battery potential of 120 V. The in-rush current i_L charging the dc bus is seen to peak at 4.8 A.

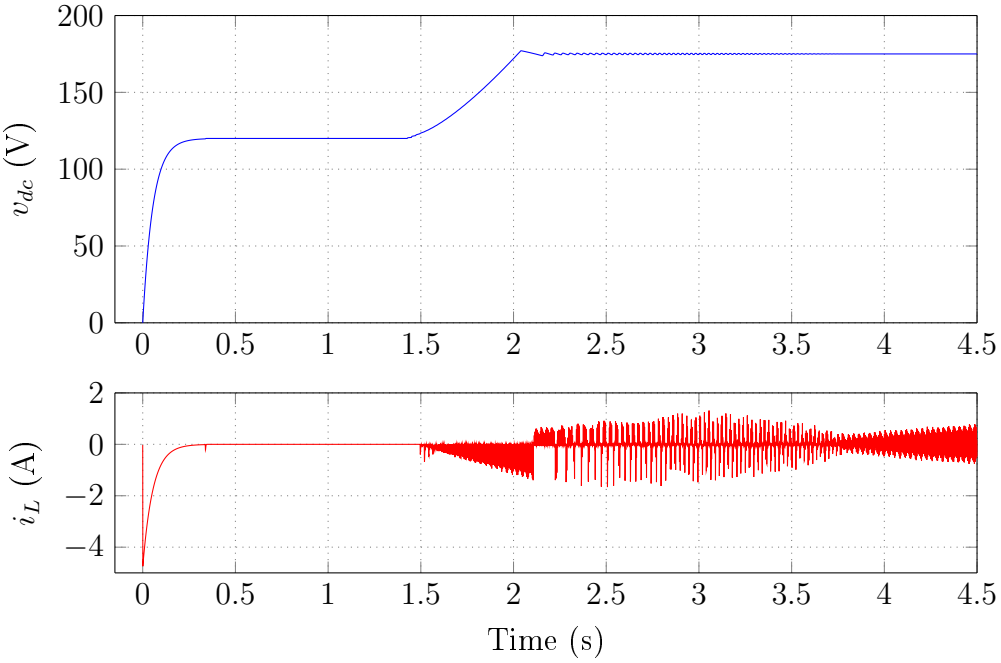

Figure 4.2: Simulated dc bus voltage and inductor current during start-up.

At approximately 1.5 s the second stage of the soft-start circuit is activated, allowing the bus voltage to rise from 120 V to 175 V over the next 0.65 seconds. When the bus voltage reaches 175 V there is a small voltage overshoot of 2 V, which is within the allowed range of 170 V to 180 V. It is thus not necessary to implement any additional anti-windup scheme [41] to prevent the dc bus voltage from overshooting after reaching its nominal value of 175 V.

The large initial ripple voltage on the dc bus is caused by the post-charge circuit limiting the on-time of the switches by adjusting the dead-time. The ripple is seen to decrease until it reaches a minimum peak-to-peak value of 27 mV once the dead-time has reached the minimum value. At time $t = 4.5$ s the dead-time has decreased sufficiently to allow the controller to function normally thus regulating the dc bus voltage to 175 V continuously without any significant voltage ripple. At the same time the inductor current is also shown to have reached the designed current ripple of approximately 2.25 A peak-to-peak.

Fig. 4.3 shows the measured dc bus voltage and inductor current during start-up. The magnitude and rate of change of the bus voltage is similar to the result of the time domain simulation shown in Fig. 4.2. Due to the sampling rate of the oscilloscope used to obtain the measurements (1000 samples over the chosen time period), the inductor current displayed in Fig. 4.3 is under sampled and thus aliasing occurs. In the 5 s measurement taken for Fig. 4.3 the inductor current is time averaged over a period of 5 ms, thus aliases of the

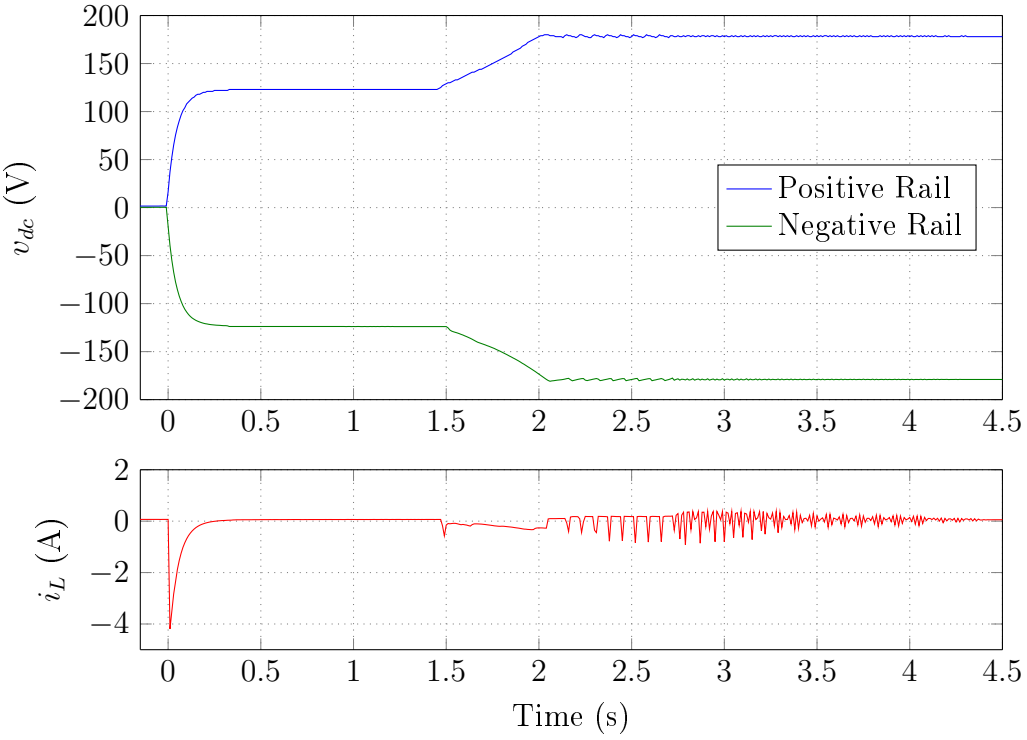

Figure 4.3: Measured dc bus voltage and inductor current during start-up.

inductor current are displayed as opposed to the true instantaneous inductor current. The inductor current ripple under normal operating conditions can therefore not be seen as in the simulated model.

As predicted, the bus voltage is observed to rise to the equivalent battery potential within 350 ms of connecting the battery to the converter at which time an audible click is heard as the relay short-circuits the soft-start resistors. The battery potential is approximately 125 V per rail section which is slightly higher than the simulated potential due to the initial state of charge of the purchased batteries. Another measurement of the start-up current i_L was taken over a 1 s time period to determine a more accurate peak start-up current of 4.6 A as shown in Fig. 4.4. The small current spike of 0.6 A at 350 ms occurs when the relay switch closes.

The bus voltage is subsequently observed to rise to and regulate at 177.2 V and -177.8 V respectively in Fig. 4.3 over a period of approximately 0.6 s as the dead-time is progressively reduced. The rail-to-rail nominal bus voltage is thus 355 V. The positive and negative dc bus voltages peak at 179 V and -180 V respectively, according to the oscilloscope measurements. This correspond to a voltage overshoot of approximately 2 V from the regulated voltage as predicted by the time domain simulation. The positive and negative bus voltage are observed to regulate 2 to 3 V higher than the nominally required value of plus

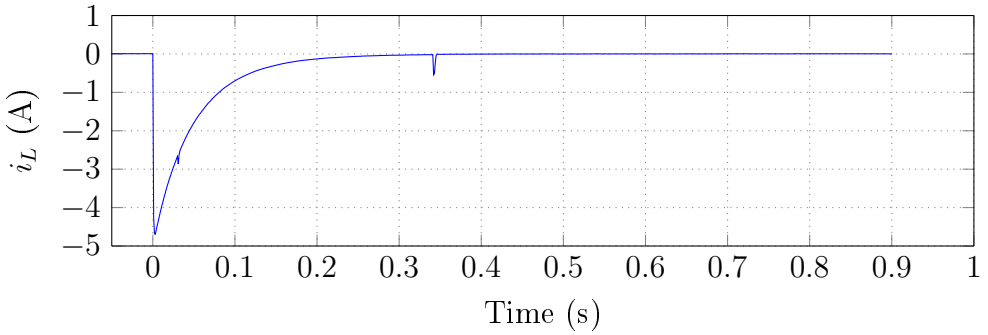

Figure 4.4: Measured inductor current during start-up.

and minus 175 V due to a small inaccuracy in the set-point value $V_{dc}{}^{*}$. Since it is still within the allowed operating range, no additional adjustments were made. After another 2.5 s the ripple on the dc bus voltage is seen to have decreased significantly and the mean inductor current is shown to be zero.

4.2.1 Gating Signal Implementation

The voltage waveform generated by the push-pull oscillator used to power the optocoupler (that communicates the gating signals between the controller and MOSFET gates) is shown in Fig. 4.5. The oscillation frequency is measured as 311 kHz. The peak-to-peak voltage is approximately 24 V corresponding to a 1:1 transformer ratio when the circuit is powered from a single 12 V battery.

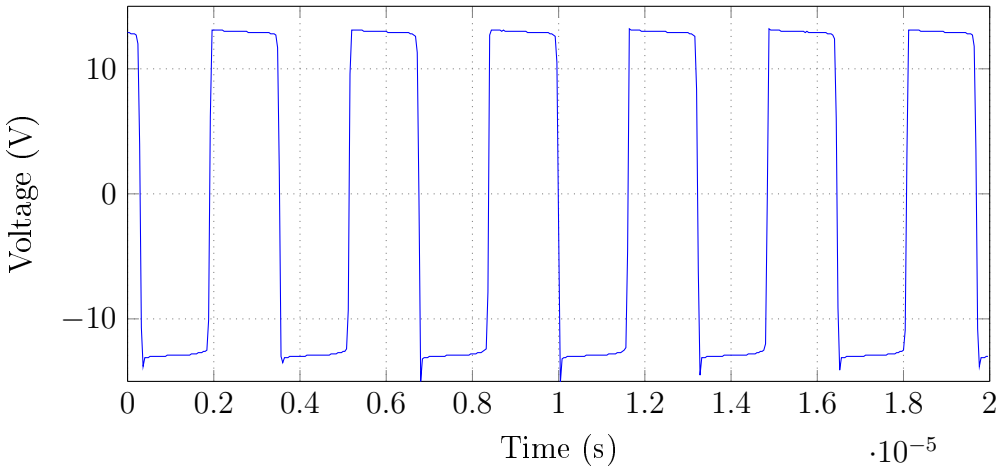

Figure 4.5: Measured oscillator signal used in gate-drive circuitry.

Both the current and voltage control loops employ integrators in their compensation amplifiers. This causes the initial modulator reference voltage (gen-

erating the PWM signals) during the start-up sequence to be at a maximum, since the dc bus voltage has not yet reached the nominal value. The duty cycle of the switches are limited to 95 %. With the dead-time included the maximum duty cycle is 92 % and the resulting gating signal generated by the comparator for Q_2 is shown in Fig. 4.6 in blue. The green line shows the signal at the gate of the MOSFET.

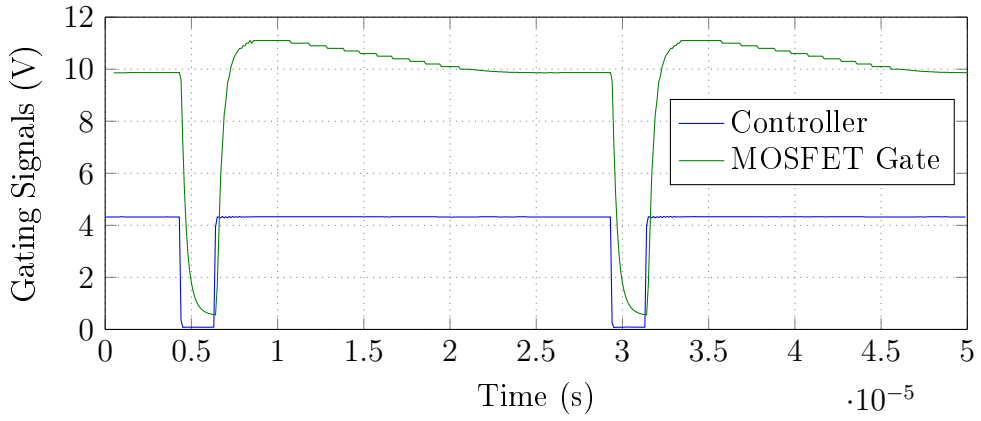

Figure 4.6: Measured gating signal from the controller and MOSFET gate for Q_2 during start-up.

A similar switching signal is seen at the gate of Q_3 while switches Q_1 and Q_4 are off completely due to the added dead-time.

4.3 Step Response

To determine the transient response of the dc-dc converter a step change in the load was implemented in both the simulated and prototype circuit. Fig. 4.7 shows the predicted response of both the dc bus voltage and inductor current to a step change in the load. The application of a 2.1 kW load was simulated by adjusting the mean dc bus current I_{dc} from 0 A to -6 A in the time domain simulation. The system is tested for a load capability slightly higher than the required 2 kW due to the availability of the 60 Ω dummy load that was used during testing. At time $t = 0.1$ s the load step response is implemented resulting in a negative average inductor current of 9.32 A and a negative voltage spike of 1.4 V. After 300 ms the simulated load is disconnected and the mean current is seen to return to zero while the dc bus voltage peaks at 176.4 V before settling back to 175 V.

A similar response is seen when a dc current source is instantly applied to the dc bus at time $t = 0.7$ s by changing the mean dc current I_{dc} from 0 A to 5.8 A (corresponding to 2.03 kW of power delivered to the converter).

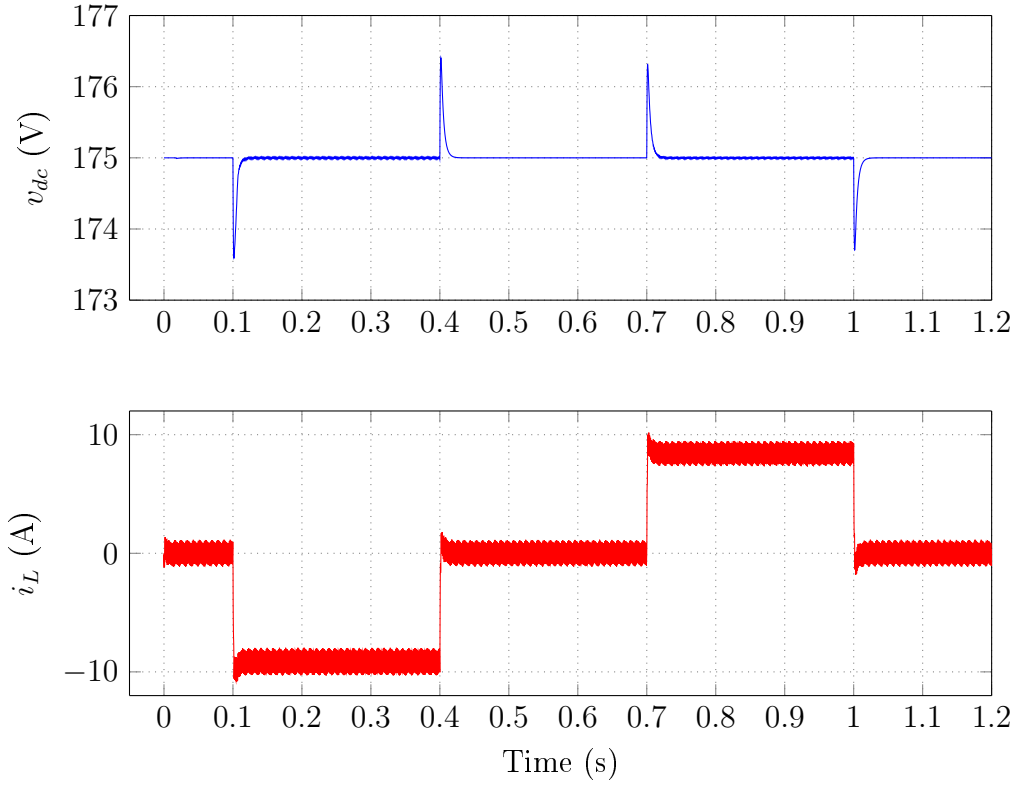

Figure 4.7: Simulated step response of dc bus voltage and inductor current.

The voltage briefly peaks at 176.3 V and the mean inductor current is shown to be 8.42 A. After 300 ms when the current source is removed, the dc bus voltage falls to 173.7 V before settling back to the nominal dc bus voltage. The inductor current is seen to return to a mean value of zero. According to the time domain simulation the duration of the transient responses are approximately 30 ms. As seen from Fig. 4.7 the simulated converter provides a good transient response by settling quickly and having a maximum voltage overshoot of less than 1 % of the nominal bus voltage. This simulation also demonstrates the bidirectional capability of the converter.

The transient response of the prototype circuit was tested by connecting and disconnecting a 2.1 kW (60 Ω) load to the 355 V nominal dc bus. The measurement was taken at the positive dc bus voltage rail by using the ac coupled setting on the oscilloscope. As shown in Fig. 4.8 the load was connected at time $t = 0.05$ s which caused a brief voltage dip of 1.32 V. The bus voltage settled back to 177.2 V after 0.5 s at which time the load was disconnected causing a voltage spike with an amplitude of 0.92 V. Another 400 ms later the dc bus voltage settled back to the nominal voltage.

The transient response of the simulated and measured step responses compare reasonable well. The main difference being the simulated circuit shows a

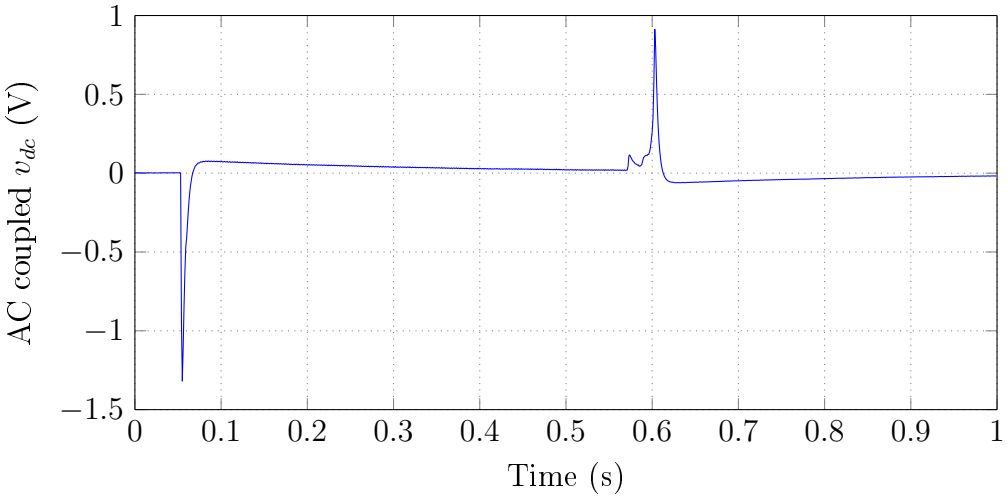

Figure 4.8: Measured step response of the dc bus voltage under ac coupling.

faster settling time than the measured step response.

The test showing the bidirectional capability of the dc-dc converter circuit will be presented in Chapter 7 as part of the system integration testing since the asynchronous generator is required to source current to the converter. The design and implementation of the inverter circuit connecting to the asynchronous generator will be discussed in the following chapters.

4.3.1 Inductor Ripple Current

The simulated inductor current ripple is shown in Fig. 4.9 and the measured inductor current at no-load is shown in Fig. 4.10. The simulation predicts a current ripple magnitude of 2.25 A peak, which is 22.5 % of absolute maximum mean current that the inductor is intended to conduct at full power (sink or source). The magnitude of the current ripple is independent of the mean current, provided that the bus voltage, battery voltage and inductance of the inductor remain constant. The inductor current duty cycle from Fig. 4.9 is shown to be 68.8 % which is as expected.

The measured inductor current at no-load has a peak-to-peak value of 2.06 A which is slightly less than the predicted value mainly due to the higher battery potential. The leakage inductance in the cables connecting the batteries to the rest of the converter circuit, as well as the leakage inductance in the path through the series connected batteries themselves will add to the total inductance causing the current ripple to decrease slightly.

The measured inductor current when a 2.1 kW load is connected across the bus rails, is shown in Fig. 4.11. The mean inductor current is -9.59 A corresponding closely to the predicted value of -9.32 A, where the negative sign indicates the batteries are sourcing instead of sinking current.

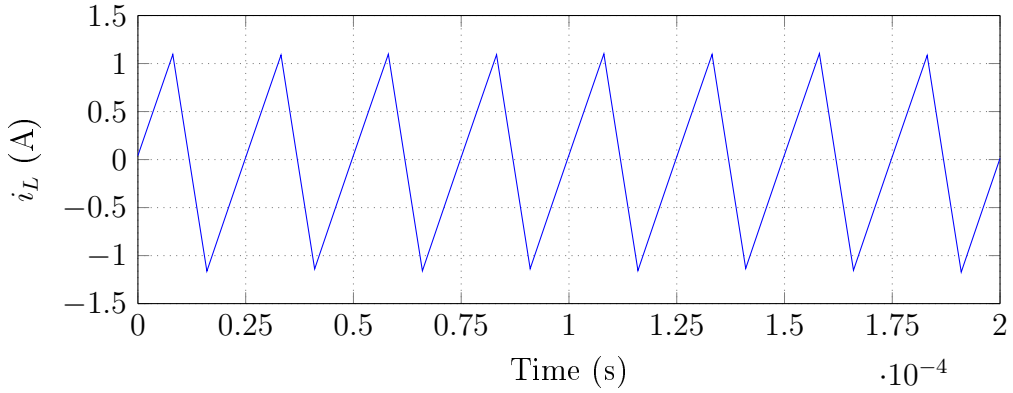

Figure 4.9: Simulated inductor current.

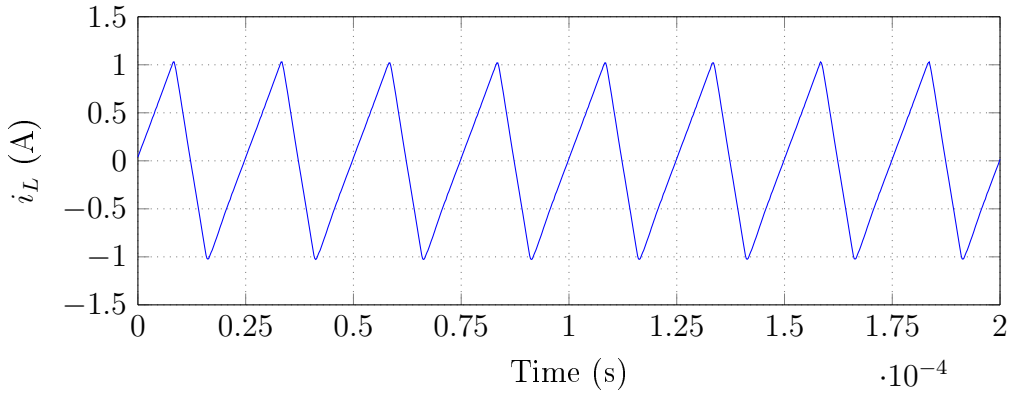

Figure 4.10: Measured inductor current without a load connected.

In the converter simulation the peak-to-peak value of the current ripple stays constant at no-load and full-load conditions since the value of the inductor and battery voltage are assumed constant. From Fig. 4.11 it can be seen that the measured peak-to-peak current ripple increased to 3.1 A at full-load, compared to the 2.06 A at zero load. This is mainly due to the drop in the total battery potential from 247.2 V to 236.6 V when the load is connected. Also there is a marginal decline in the inductance of the inductor, due to the decreased instantaneous permeability of the inductor core material at greater magnetisation.

In both cases, the measured current is of triangular form with a duty cycle of approximately 69 % at no-load and a duty cycle of 66 % at full-load, during which time switches Q_1 and Q_4 are turned on and the inductor current is observed to increase linearly.

Overall, the time domain simulations and measurements for the dc-dc converter correspond very well. The simulation can thus be considered a useful

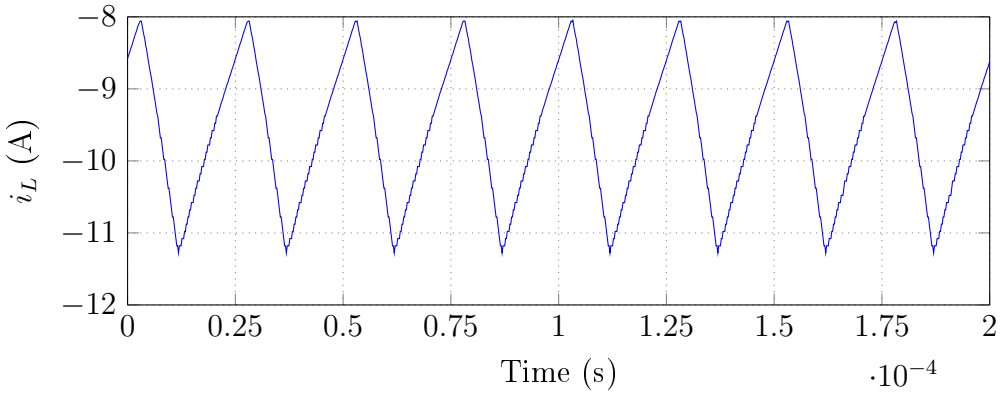

Figure 4.11: Measured inductor current with a 2.1 kW load connected to the dc bus rails.

tool for predicting the behaviour of the prototype circuit.

4.3.2 Gating Signals

The measured controller gating signals for switches Q_1 and Q_2 under no-load are presented in Fig. 4.12. The switches are seen to never be on simultaneously indicating the dead-time of 1 μs was implemented correctly. The duty cycle of switch Q_1 is 69.2 % and 22.7 % for Q_2.

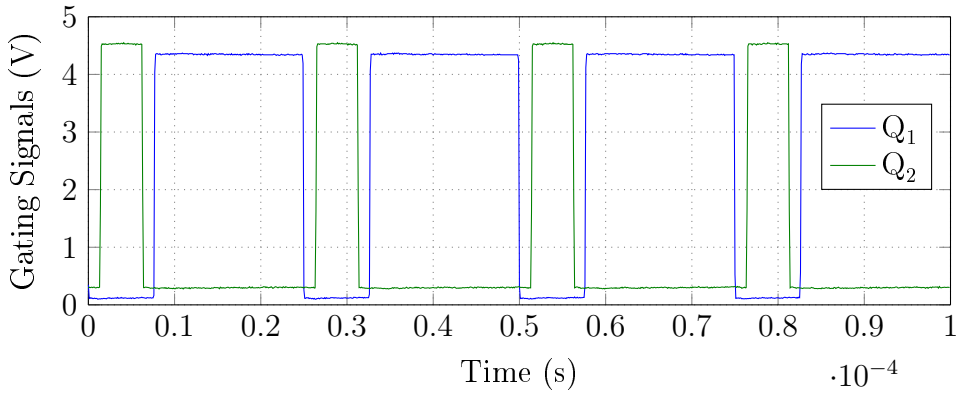

Figure 4.12: Measured controller gating signals for Q_1 and Q_2 under steady-state no-load conditions.

4.4 Efficiency

A 60 Ω resistor bank was employed to load the converter to approximately 2.1 kW. The converter efficiency is determined by comparing the power delivered to the load to that drawn from the battery. The measured instantaneous inductor current and ac coupled battery voltage are shown in Fig. 4.13. The mean battery voltage was measured using a multimeter as 236.6 V. The instantaneous input power is also shown in Fig. 4.13 and was obtained by multiplying the magnitude of the inductor current with the battery voltage (after adding the dc offset of 236.6 V), using MATLAB.

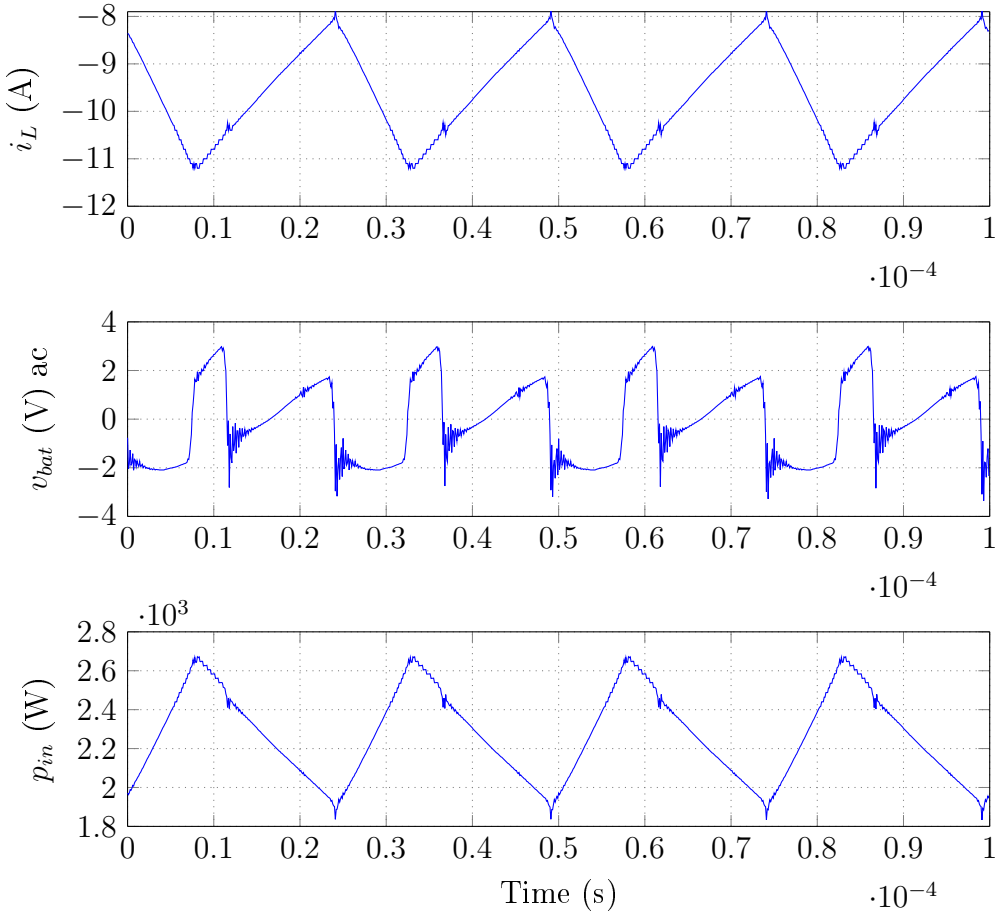

Figure 4.13: Measured inductor current and ac coupled battery voltage under load.

From Fig. 4.13 the measured ac coupled battery voltage is seen to be in phase with the measured inductor current. Since there is no phase shift between the battery voltage and inductor current, the average inductor and battery voltage can be used to calculate the average input power. With the average inductor

current measured with a LEM current probe as 9.592 A, the average input power is thus

$$P_{in} = V_{bat} I_L = 2269 \text{ W}. \tag{4.1}$$

The mean value of the instantaneous input power p_{in} shown in Fig. 4.13 was calculated in MATLAB as 2268.6 W confirming the average power calculation of (4.1).

The regulated dc bus voltage was measured with another multimeter as 355 V rail-to-rail and the dc bus current flowing into the load was measured with the LEM current probe as 6.01 A. The output power at the load is thus

$$P_{out} = V_{dc} I_{dc} = 2133 \text{ W}, \tag{4.2}$$

resulting in a converter efficiency of

$$\eta = \frac{P_{out}}{P_{in}} = 94.02\%. \tag{4.3}$$

The total power loss is calculated as

$$P_{loss} = P_{in} - P_{out} = 136 \text{ W}. \tag{4.4}$$

The total switching and conduction losses were calculated as 14.33 W in (3.28) for one half-bridge converter, thus 28.66 W for the complete converter circuit. The current sense resistors of 68 mΩ is responsible for a power loss of 6.3 W at a mean inductor current of 9.6 A. The remaining power loss of a 101 W is mainly due to the battery's internal resistance, the inductor's equivalent series resistance and the resistance within the (long) cables connecting the batteries to the dc-dc converter circuit.

4.5 Summary

The time domain simulation of the dc-dc converter circuit was presented in this chapter along with the measured test results. The test set-up was described in detail. The simulated start-up response of the dc-dc converter compared extremely well to the measured start-up response. The transient response of the prototype circuit was tested by implementing a step change in the load connected to the converter's dc bus terminals. The simulated and measured transient responses compared reasonable well. The dc-dc converter circuit demonstrated its ability to regulate the dc bus voltage under no-load and loaded conditions, whilst meeting the design specifications. The prototype circuit showed a high efficiency and overall satisfactory performance.

Chapter 5

Asynchronous Machine Modelling

An asynchronous machine is used as the generator that connects to the inverter circuit functioning in rectifier mode. A model of the asynchronous machine is required in order to design the controller for the inverter and generator. This chapter derives all the necessary machine parameters for a computer simulated machine model. The machine model is demonstrated and compared with the true machine characteristics.

5.1 Machine Parameter Estimation

The asynchronous machine used is a 3 kW three-phase squirrel-cage rotor induction motor. The motor will however be operated as a generator. The equivalent circuit for an asynchronous machine (also known as an induction machine) was described in detail in the literature review Section 2.4.2. The equivalent per-phase circuit diagram is repeated here as shown in Fig. 5.1 for convenience.

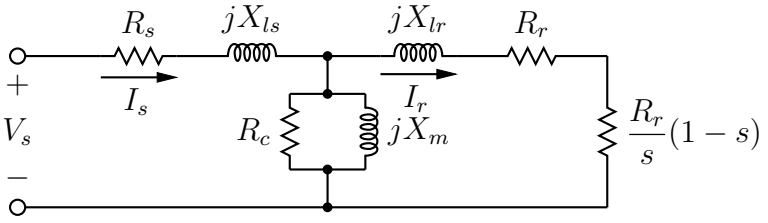

Figure 5.1: Per-phase equivalent circuit of an induction machine.

The equivalent circuit parameters can be obtained by measurements, no-load testing and a locked-rotor test. The datasheet provides most of the no-load and locked-rotor measurements required for the parameter estimation calculations. Table 5.1 provides a summary of the machine characteristics, as given in the datasheet.

Table 5.1: Three phase induction machine characteristic values.

Parameter	Rated Value
Shaft power	3 kW
Frequency	50 Hz
Poles	2
Slip	4.33 %
Voltage	230/400 V (ac rms)
Current	10.6/6.07 A
Locked rotor current	70.7/40.7 A
No-load current	4.87/2.8 A
Full load torque	9.99 Nm
Locked rotor torque	230 %
Breakdown torque	280 %

Due to the available bus voltage of ± 175 V provided by the dc-dc converter, the induction machine will be connected in delta (low-voltage configuration). The machine slip is denoted by a small letter s for the duration of this chapter.

5.1.1 Stator Resistance

The stator resistance R_s shown in Fig. 5.1 was measured with a multimeter as 2.1 Ω by measuring the resistance between one of the stator terminals and neutral, while the machine was connected in wye configuration.

5.1.2 Leakage Reactance

The leakage reactances X_{ls} and X_{lr} shown in Fig. 5.1 are usually calculated as one entity X_e and approximated by

$$X_{ls} = 0.4\ X_e, \tag{5.1}$$

and

$$X_{lr} = 0.6\ X_e, \tag{5.2}$$

for a class B motor [26] such as the motor used for this project. An approximate model of the per-phase equivalent circuit [27] of an induction machine is used to determine the leakage reactances as shown in Fig. 5.2. The approximation is valid since the core resistance R_c and impedance of the magnetising inductance X_m are much larger than the stator leakage impedance $R_s + jX_{ls}$.

The leakage reactances are calculated from the expression for breakdown torque which is derived below. First consider the expression for the real power developed at the shaft of the machine as given in (2.32) and repeated here:

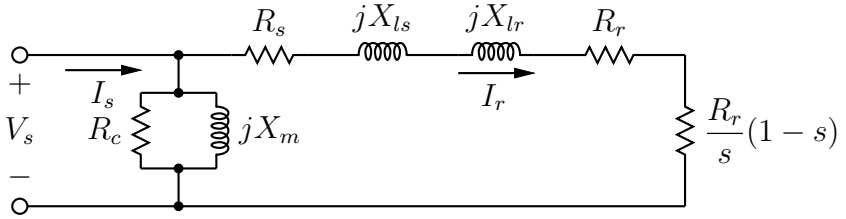

Figure 5.2: Approximate per-phase equivalent circuit of an induction machine.

$$P_d = 3{I_r}^2 R_r \left(\frac{1-s}{s}\right). \tag{5.3}$$

The rotor current I_r is calculated as

$$I_r = \frac{V_s}{R_e + jX_e + R_r\frac{(1-s)}{s}}, \tag{5.4}$$

where

$$R_e = R_s + R_r. \tag{5.5}$$

Substituting (5.4) into (5.3) results in

$$P_d = \frac{3V_s^2 R_r \frac{(1-s)}{s}}{R_e^2 + X_e^2 + \left[R_r\frac{(1-s)}{s}\right]^2 + 2R_e R_r \frac{(1-s)}{s}}. \tag{5.6}$$

The torque is related to power by the synchronous angular velocity ω_s as given in (2.33) which results in a developed shaft torque of

$$T_d = \frac{1}{\omega_s}\left[\frac{3V_s^2 \frac{R_r}{s}}{R_e^2 + X_e^2 + \left[R_r\frac{(1-s)}{s}\right]^2 + 2R_e R_r \frac{(1-s)}{s}}\right]. \tag{5.7}$$

As seen from (5.7) the maximum torque, also known as the breakdown torque, occurs when $\frac{1-s}{s}$ is at a minimum. The breakdown slip s_b is obtained by differentiating (5.7) with respect to s and setting it equal to zero which results in

$$s_b = \frac{R_r}{\sqrt{R_s^2 + X_e^2}}. \tag{5.8}$$

The expression for the breakdown torque T_{dm} is calculated by substituting (5.8) into (5.7) resulting in

$$T_{dm} = \frac{3V_s^2}{2\omega_s}\left[\frac{1}{R_s + \sqrt{R_s^2 + X_e^2}}\right]. \tag{5.9}$$

From (5.9), the measured stator resistance and the values given in Table 5.1, the combined leakage reactance X_e is calculated as 6.60 Ω. The individual leakage reactances are calculated from (5.1) and (5.2) as $X_{ls} = 2.64\ \Omega$ and $X_{lr} = 3.96\ \Omega$ respectively.

5.1.3 Rotor Resistance

The rotor resistance R_r (referred from the rotor to the stator) is calculated from the developed power expression given in (5.6) as 1.96 Ω.

5.1.4 Magnetising Reactance

The magnetising reactance X_m is calculated from the no-load test. At no-load the slip is almost zero and hence the impedance of the rotor is almost infinite. Fig. 5.2 thus reduces to Fig. 5.3.

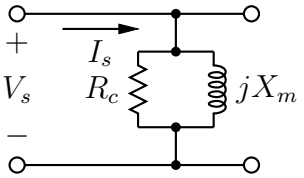

Figure 5.3: Reduced equivalent circuit of an induction machine under no-load.

The magnetising reactance is given by

$$X_m = \frac{V_{nl}^2}{Q_{nl}}, \tag{5.10}$$

where

$$Q_{nl} = V_{nl} I_{nl} \sin(\theta_{pf}). \tag{5.11}$$

The no-load current is given in the datasheet as 2.8 A and the no-load voltage is the same as the rated voltage, 230 V. The power factor at no-load is given in the datasheet as 0.15. The power factor angle at no-load is thus

$$\theta_{pf} = \cos^{-1}(0.15) = 81.37^\circ \tag{5.12}$$

Substituting (5.11) and (5.12) into (5.10) results in

$$X_m = \frac{V_{nl}}{I_{nl} \sin(\theta_{pf})} = 83.08\ \Omega. \tag{5.13}$$

5.1.5 Core Resistance

The core resistance R_c is calculated in a similar manner as the magnetising inductance. With reference to Fig. 5.3 the core resistance is

$$R_c = \frac{V_{nl}^2}{P_{nl}}, \tag{5.14}$$

where

$$P_{nl} = V_{nl} I_{nl} \cos(\theta_{pf}). \tag{5.15}$$

The resulting core resistance R_c is calculated as 547.6 Ω. The calculated machine parameters are summarised in Table 5.2

Table 5.2: Calculated machine parameters.

Parameter	Value
R_s	2.1 Ω
X_{ls}	2.64 Ω
X_{lr}	3.96 Ω
R_r	1.96 Ω
X_m	83.08 Ω
R_c	547.6 Ω

5.2 Machine Characteristics

The characteristic curves related to slip are given in the machine datasheet and are used to determine the accuracy of the machine model. Since the machine is rated to operate at 50 Hz all the machine data given in the datasheet is at a stator frequency of 50 Hz. The voltage applied to stator phases are considered to have a constant rms value of 230 V.

5.2.1 Torque-Speed Relationship

The modelled and measured datasheet torque-speed curves are shown in Fig. 5.4. From the datasheet curve, the rotor speed is given as a percentage of the rated speed (50 Hz, 3000 rpm), thus the developed torque is given for slip values ranging from 0 to 1. If the rotor speed is equal to the rated stator speed then the slip is 0, and if the rotor speed is zero the slip is 1. The modelled torque curve was produced by simulating the developed torque as given in (5.7) for slip values also ranging from 0 to 1.

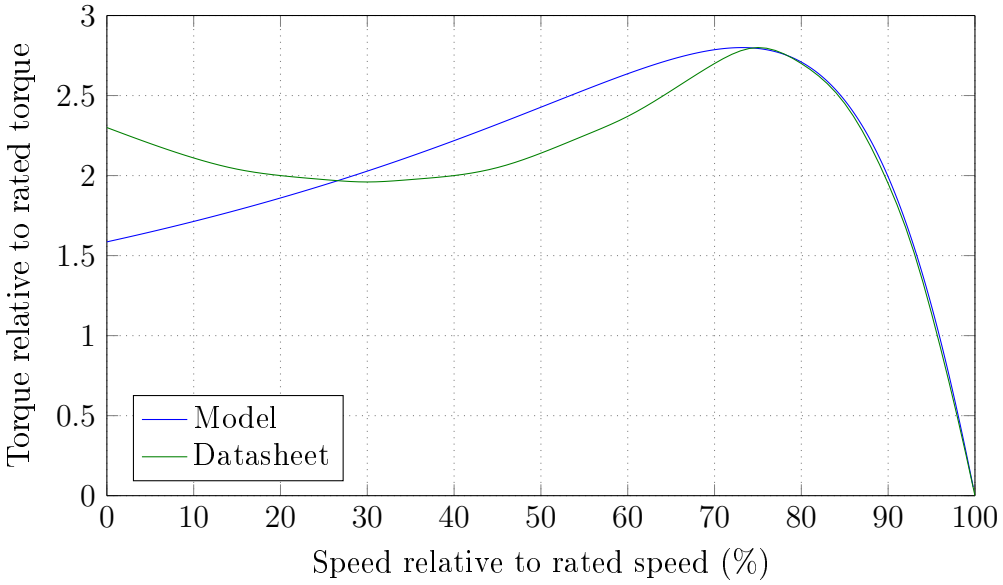

Figure 5.4: Torque vs rated speed characteristic curve.

To achieve the modelled curve of Fig. 5.4 the rotor resistance was changed from the calculated value of 1.96 Ω to 1.86 Ω, and the magnetising inductance was slightly reduced to 80 Ω. As seen from Fig. 5.4 the modelled curve only resembles the curve given in the datasheet from 0 % slip to 25 % slip. The equivalent model is thus not able to predict an accurate torque response for slip values greater than 25 %, at which point the breakdown torque is reached. Since the induction machine will never operate continuously at slip values greater than a few percent, the model need only be accurate for slip values ranging from 0 % to approximately 6 %. The rated machine slip is 4.33 % and thus the machine will not operate at more than one or two percent slip above the rated slip continuously.

The torque-speed curve shown is for motor operation where power is delivered to the shaft. Since the induction machine will be used as a generator, the machine will be modelled using negative slip values.

5.2.2 Current-Speed Relationship

Similarly the stator current related to the rated speed is shown in Fig. 5.5 for both the modelled and measured (from the datasheet) case. The modelled stator current was calculated from Fig. 5.1 as

$$I_s = \left| \frac{V_s}{Z_{eq}} \right|, \tag{5.16}$$

where

$$\begin{aligned} Z_{eq} &= R_s + jX_{ls} + R_c||jX_m|| \left(jX_{lr} + \frac{R_r}{s}\right) \\ &= R_s + jX_{ls} + \frac{R_c jX_m \left(jX_{lr} + \frac{R_r}{s}\right)}{R_c jX_m + (R_c + jX_m)\left(jX_{lr} + \frac{R_r}{s}\right)}. \end{aligned} \tag{5.17}$$

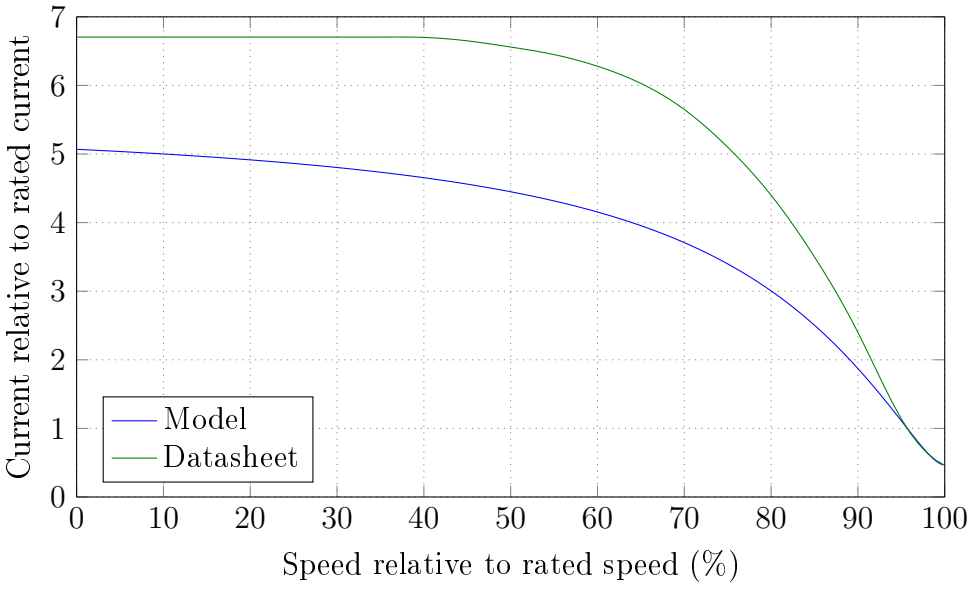

Figure 5.5: Stator current vs rated speed characteristic curve.

The modelled current is seen to deviate significantly more from the measured current for slip values greater than 6 %. For small slip values the model does however correspond to the current given in the datasheet curve.

Since the measured current and torque curves deviate from the modelled curves, it is clear that the values of the machine parameters also change at different slip values. The locked-rotor test for instance is only performed for a few seconds during which time the machine heats up significantly. A change in temperature is known to change the effective resistance. The rotor resistance may vary 50 % up to a 100 % from the nominal value at rated slip due to heating [42]. The magnetising inductance will vary due to flux saturation at high slip values. The leakage reactances change as the stator and rotor currents change due to the non-linear behaviour of magnetic materials at higher field-intensity values (which is directly related to current) [43].

The equivalent circuit parameters determined in this chapter are thus adequate to predict the behaviour of the chosen induction machine at very low slip values (less than 6 % slip).

5.3 Dynamic Machine Model

The dynamic d-q model of an asynchronous (or induction) machine was already discussed in Section 2.4.3. This model, consisting of equations (2.38) to (2.47), is used to model the dynamic behaviour of the 3 kW induction machine described in this chapter at low slip values. The final machine parameters used for modelling are summarised in Table 5.3. The core resistance R_c is not taken into account for this model.

Table 5.3: Machine parameters used for modelling.

Parameter	Value
R_s	2.1 Ω
X_{ls}	2.64 Ω
X_{lr}	3.96 Ω
R_r	1.86 Ω
X_m	80 Ω

Negative slip values are used to simulate generator operation. The machine model was programmed in a MATLAB script where the differential equations were solved using the iterative Euler method.

5.3.1 Modelling Results

The simulation was tested at a slip of zero to confirm the behaviour of the dynamic machine model. At a slip of zero the no-load current is given as 2.8 A in the datasheet and thus a similar value is expected for the model. Three sinusoidal 50 Hz, 230 V rms voltages phase shifted by 120° from each other were applied to the dynamic model and the simulation results are shown in Fig. 5.6.

The stator voltages were programmed to increase linearly over a time period of 0.16 s before reaching a nominal value of 230 V rms. Although this did reduce current surges during start-up, to avoid any overcurrent conditions altogether, the stator voltages have to increase linearly over a time period of approximately 2 s. Once the current settled it reached a steady-state value of 2.78 A rms which is close to the true no-load current of 2.8 A. Under steady-state no-load conditions the model showed a developed torque of zero as expected.

Given that the generator will operate at a slip value of around -5 %, another simulation was conducted to confirm the generator operation of the dynamic model. The resulting stator and rotor currents for one of the three phases are shown in Fig. 5.7. The rotor shaft was modelled to rotate at a constant angular velocity of 50 Hz.

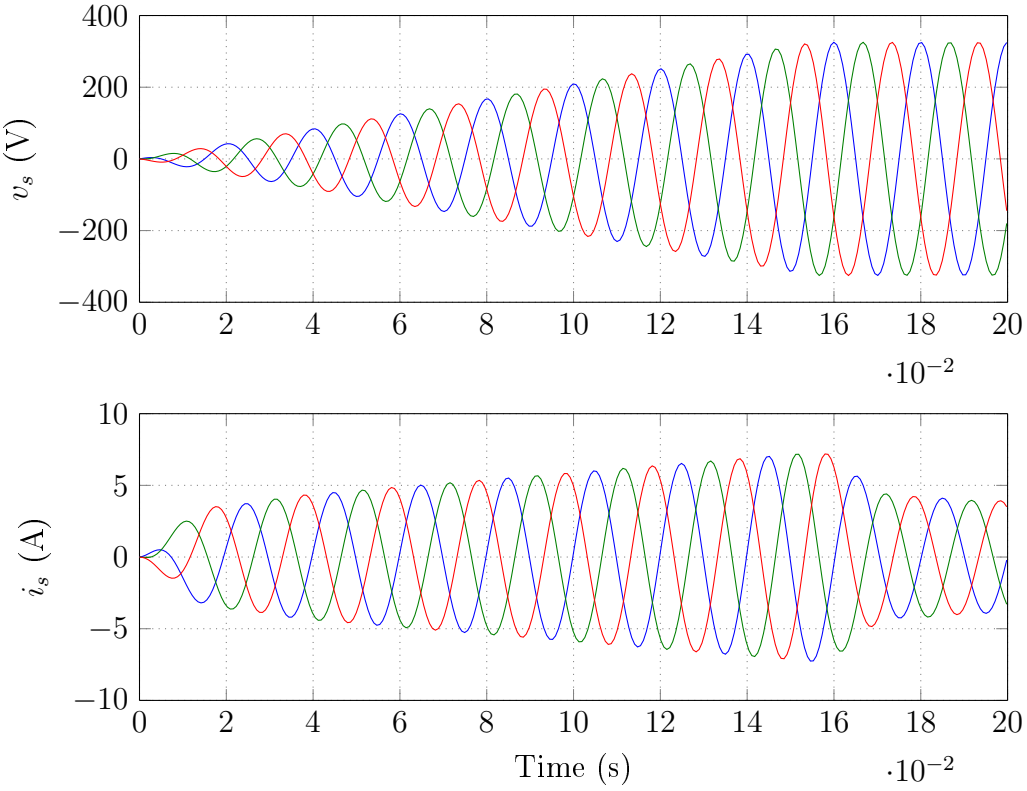

Figure 5.6: Three-phase stator voltages and currents at zero slip.

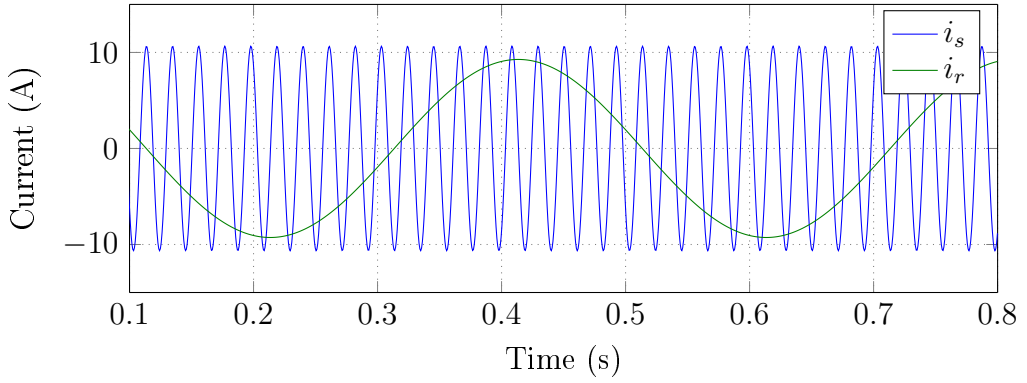

Figure 5.7: Stator and rotor currents at -5 % slip.

The stator current is shown to have a frequency of 47.62 Hz while the rotor current has a frequency of 2.38 Hz corresponding to a slip of 5 %. The developed torque of the machine is -15.27 Nm according to the simulation, indicating that 15.27 Nm of torque must be applied to the shaft in order to achieve -5 % slip operation.

5.4 Summary

This chapter derived the asynchronous generator machine parameters from the equivalent machine model and datasheet information. The machine model was simulated and the results compared to the given datasheet information to confirm the credibility of the model. The model was shown to be reasonably accurate for low slip values. The generator operation of the machine was also investigated. The next chapter contains the design of the inverter control circuit which is based on the machine parameters and performance detailed in this chapter.

Chapter 6

Inverter Design and Implementation

The design and implementation of a non-isolated bidirectional current-controlled switched-mode inverter functioning as a synchronous rectifier is described in this chapter. The inverter connects to the dc bus provided by the dc-dc converter presented in Chapters 3 and 4. The asynchronous generator described in Chapter 5 is used to supply power to the dc bus through the inverter circuit.

The generator is required to supply a maximum of 2 kW of electrical power to a load connected between the dc bus rails, or if a load is not present, to the dc-dc converter in order to charge the converter's batteries. The voltages applied to the generator stator terminals are controlled as a function of the dc bus current and the dc-dc converter's battery voltage. Two control loops are used to facilitate the regulation of the battery voltage. The design of the control loops are presented along with their closed-loop stability analysis. The design and implementation of various additional safety features are also described.

6.1 Basic Circuit Operation

The inverter circuit is used to regulate the dc-dc converter battery voltage to ensure the batteries are kept at their optimal floating use voltage of 13.6 V each. The positive and negative dc-dc converter bus rails, $+V_{dc}$ and $-V_{dc}$, connect to the inverter terminals. The complete circuit diagram of the inverter circuit connected to the already designed dc-dc converter circuit is shown in Fig. 6.1.

The inverter circuit is based on the commonly used three-phase half-bridge topology, as shown in Fig. 6.1, with freewheeling diodes connected across the switches. The current is assumed to flow into the dc bus thus indicating the three-phase machine is operating as a generator and the inverter as a synchronous rectifier.

The dc bus terminals of the inverter and converter are connected together

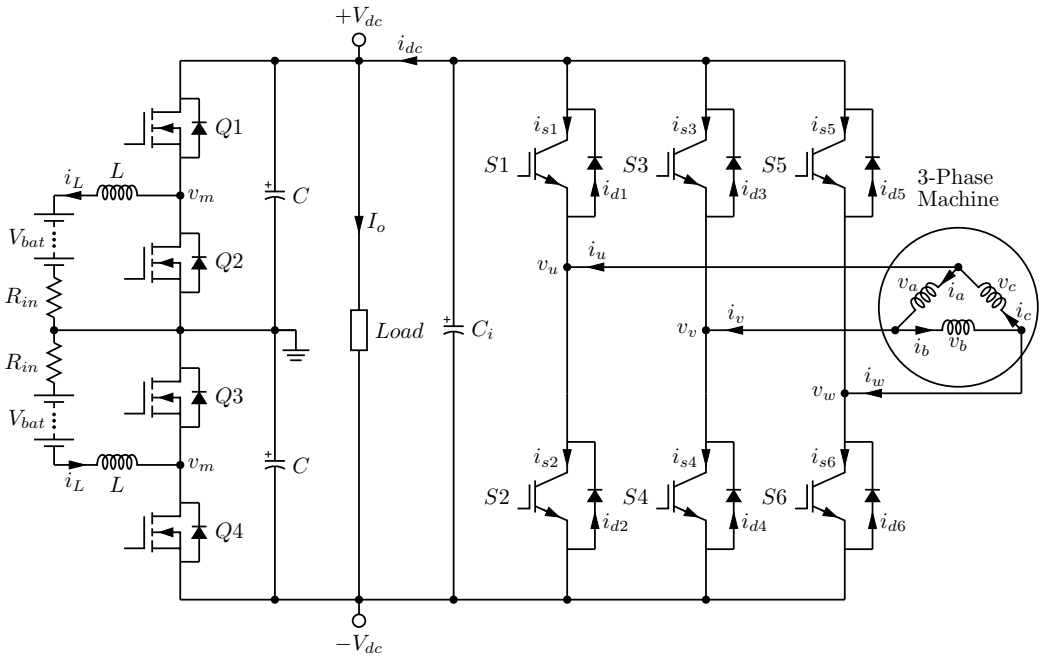

Figure 6.1: Bidirectional converter and inverter interface circuit.

by means of multi-strand wires. The wires are about 1 m long. A load can also be connected to the dc bus if desired. A 100 μF 400 V electrolytic capacitor is connected in parallel with a 100 nF 400 V ceramic capacitor and the combined capacitance is denoted C_i in Fig 6.1. The capacitors are connected between the dc bus rails on the inverter side to filter any possible high-frequency noise due to the inductance of the wire connection.

The dc-dc converter regulates the dc bus voltage to 355 V rail-to-rail. The positive denoted dc bus current i_{dc} is regulated and limited to a maximum mean value of 5.7 A by the inverter's control circuit. This permits a power transfer of up to 2023 W from the generator to the nominal 355 V dc bus, thus meeting the power requirement of 2 kW. Since the speed of the generator shaft varies, as would be the case with an air-driven turbine generator, the maximum electrical power that can be drawn from the generator is dictated by the mechanical power applied to the generator shaft at a given shaft speed. The current in the generator windings should never exceed the rated generator current, regardless of the generator shaft speed.

The magnitude and frequency of the fundamental voltages (v_{uf}, v_{vf} and v_{wf}) applied to the generator stator terminals are controlled to maintain a constant Volt/Hertz ratio. Note all subscripts ending with an f indicate the fundamental component of said waveform. A constant Volt/Hertz ratio corresponds to a constant rms flux within the machine, since flux is proportional to voltage integrated with respect to time. If constant flux is not maintained, the magnetic core of the machine will saturate causing large saturation currents

to flow which can damage the machine.

The voltages applied to the generator stator terminals, v_u, v_v and v_w, are produced by the inverter circuit. An IGBT module containing six IGBTs with freewheeling diodes included, are used for switches S_1 through S_6. The generation of the PWM signals controlling the six switches are shown in Fig. 6.2 in block diagram form.

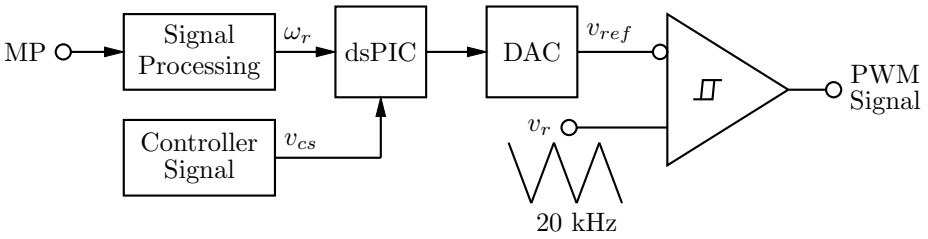

Figure 6.2: PWM signal generation block diagram.

The control circuit of the inverter produces three sinusoidal modulator reference voltages, denoted v_{ref} in Fig. 6.2, each separated 120 degrees from each other with equal magnitude. The control circuit includes a dsPIC digital signal controller and a digital-to-analog converter (DAC) to generate these reference voltages as shown in Fig. 6.2.

The speed at which the generator shaft is rotating ω_r is measured using a magnetic pick-up. The output signal from the magnetic pick-up, denoted MP in Fig. 6.2, is processed and given as an input to the dsPIC. The generator is designed to function at a constant negative slip of -5.47 % and thus the frequencies of the modulator reference voltages are approximately 5 % lower than the measured shaft speed.

The amplitudes of the modulator reference voltages are dependent upon the analog control signal v_{cs}, feeding into the dsPIC as shown in Fig. 6.2, as well as the speed of the generator shaft ω_r. The control signal v_{cs} is generated by the compensation amplifier located inside the inverter's inner control loop and is described in more detail in the next section. The amplitudes of the reference voltages are scaled according to the magnitude of v_{cs} and the speed input ω_r in order to maintain constant rms flux within the generator.

The modulator reference voltages are compared to a triangular carrier waveform v_r with a chosen frequency f_s of 20 kHz to generate the PWM switching signals as shown in Fig. 6.2. The top and bottom switches of each of the three half-bridge legs switch complementary to each other. With reference to Fig. 6.1, when one of the top switches S_1, S_3 or S_5 is switched on, the respective pole voltage is pulled high to $+V_{dc}$. Similarly, when one of the bottom switches S_2, S_4 or S_6 is switched on, the respective pole voltage is pulled low to $-V_{dc}$.

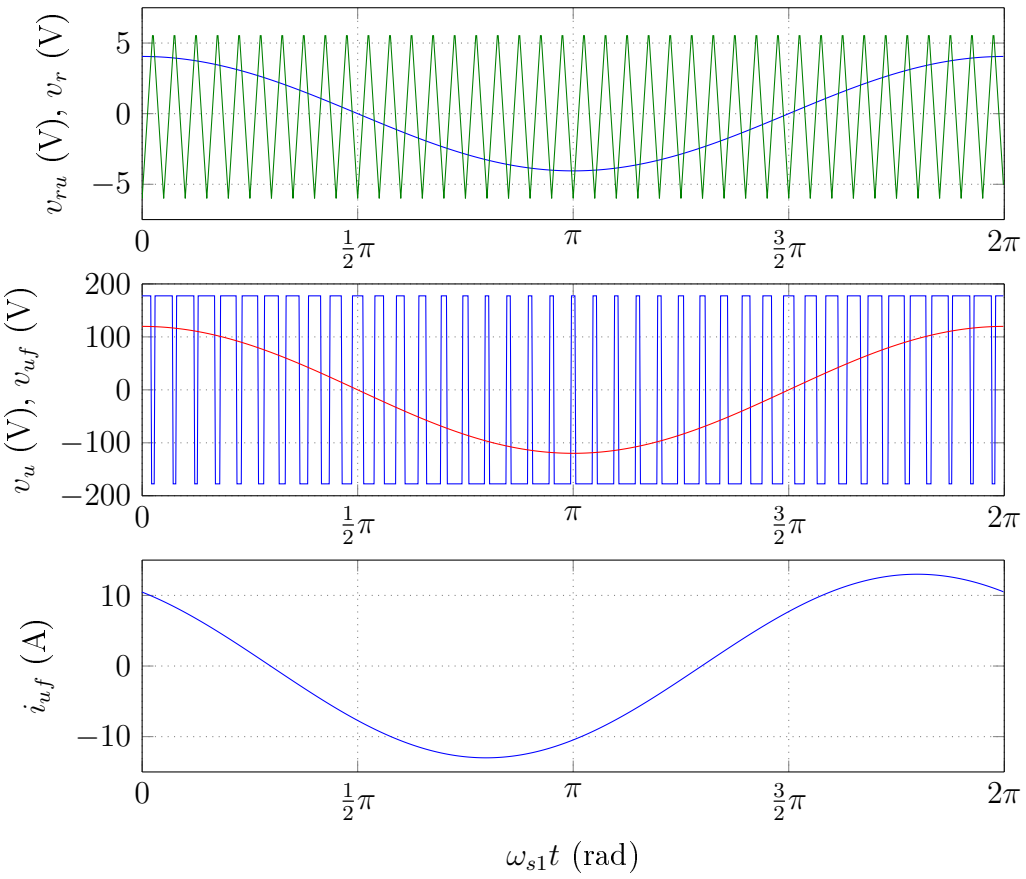

Figure 6.3: Inverter phase voltage and current for one half-bridge circuit.

Figure 6.3 illustrates the operation of the inverter circuit for the half-bridge with the pole voltage v_u. It should be noted that the triangular carrier waveform v_r shown in green in Fig. 6.3 has a frequency 2 kHz instead of the designed 20 kHz frequency simply to allow a more detailed viewing of the circuit operation in which the switching action can clearly be seen. The first plot shows the corresponding modulator reference voltage v_{ru} generated by the control circuitry and is defined as

$$v_{ru} = V_c \cos(\omega_{s1} t), \tag{6.1}$$

where V_c is the dsPIC scaled amplitude of the modulator reference voltage and ω_{s1} is the angular frequency of the modulator reference voltage. The time period for one complete angular rotation of 2π is defined as T_1. The angular frequency w_{s1}, and thus also the time period T_1, will vary due to the variable speed of the generator shaft. The reference voltage v_{ru} is thus used to modulate the phase voltage v_u and the amplitude modulation index m_a is given by [11]

$$m_a = \frac{V_c}{V_r}, \tag{6.2}$$

where V_r is the amplitude of the triangular carrier waveform v_r. The carrier waveform is generated in an identical manner to the carrier waveform used in the converter control circuit detailed in Section 3.2.1. The only difference is a 2 MHz crystal (instead of a 4 MHz crystal) is used to produce the 20 kHz triangular switching signal. The peak-to-peak output voltage of the triangular waveform v_r is 12 V, thus V_r equals 6 V. The amplitude V_c of each of the modulator reference voltages is limited to 5 V resulting in a maximum modulation index of

$$m_a = \frac{V_c}{V_r} = \frac{5}{6} = 0.833. \tag{6.3}$$

The second plot in Fig. 6.3 shows the modulated phase voltage v_u in blue and the fundamental component v_{uf} of the voltage in red. No filter is added between the inverter pole points and the stator terminals; hence the modulated phase voltages are applied directly to the generator stator terminals. The induction machine does not require filtered voltages at its stator terminals since the internal machine inductance is very high and thus the machine acts as a filter in itself. This property is described in more detail in the next subsection.

In Fig. 6.3 the fundamental phase voltage v_{uf} is shown to be in phase with the modulator reference signal v_{ru}. The amplitude V_p of the fundamental waveform v_{uf} is thus related to the modulation index by

$$V_p = m_a \frac{V_{dc(pp)}}{2}, \tag{6.4}$$

where $V_{dc(pp)}$ is the peak-to-peak dc bus voltage of 355 V. The waveform v_{uf} is thus given by

$$v_{uf} = V_p \cos(\omega_{s1} t). \tag{6.5}$$

The third plot in Fig. 6.3 shows the fundamental component i_{uf} of the phase current i_u to demonstrate the phase shift between the fundamental phase voltage v_{uf} and current i_{uf}. This phase shift is due primarily to the inductance of the generator and is calculated from the impedance of the generator. With the generator parameters determined in the previous chapter, the impedance Z_{eq} between two stator terminals is calculated using (5.17) as

$$Z_{eq} = 31.46 \angle 143.62^\circ\ \Omega, \tag{6.6}$$

at an angular frequency of 50 Hz. The fundamental phase voltage v_{uf} is used as the reference waveform. With reference to (6.6) and with the phase currents defined as positive when flowing out of generator and into the dc

bus, the current is calculated as leading the reference voltage by $\phi = 36.38°$. The amplitude of the fundamental phase current is defined as I_p, hence the fundamental phase current i_{uf} is given by

$$i_{uf} = I_p \cos(\omega_{s1} t + \phi). \tag{6.7}$$

The corresponding currents through switches S_1 and S_2 are shown in Fig. 6.4 with reference to Fig. 6.1 and Fig. 6.3, where current is defined as positive when flowing from the generator into the dc bus. During the positive half-cycle of i_{uf} shown in Fig. 6.3 and while switch S_2 is off, current will flow from the generator through the forward biased diode of S_1 towards the dc bus. When switch S_2 is on current will flow through the IGBT of S_2 as shown in Fig 6.4.

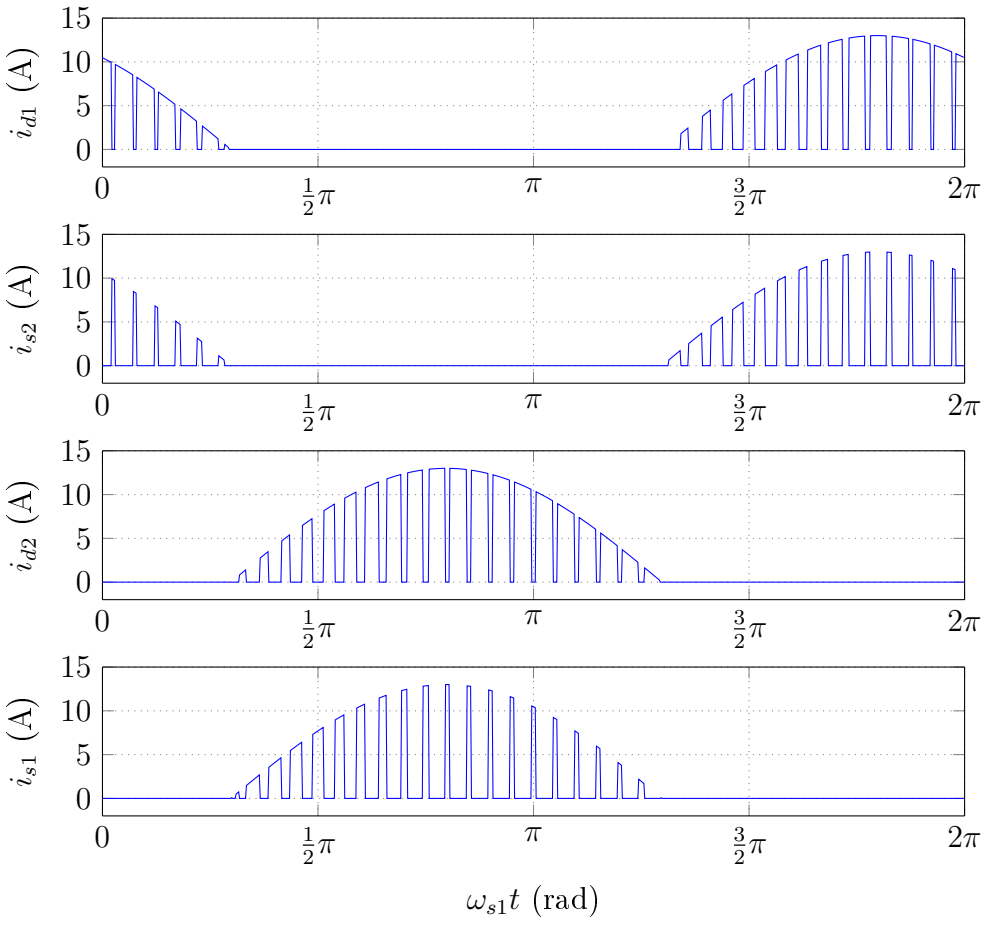

Figure 6.4: Switch and diode currents for S_1 and S_2 over a single angular rotation.

During the negative half-cycle of i_{uf} current will flow from the dc bus towards the generator through the IGBT of S_1 as long as switch S_1 is on. However,

when switch S_1 is off and i_{uf} is still within the negative half-cycle, current will flow through the forward biased diode of S_2.

The time-varying duty cycle of switch S_1 is related to the modulation index given in (6.2) and the modulator reference voltage v_{ru} defined in (6.1) such that [31]

$$d_1 = \frac{1}{2}\left[1 + m_a \cos(\omega_{s1} t)\right]. \tag{6.8}$$

The duty cycle d_1 is thus out of phase with i_{uf} as seen from Fig. 6.4. The instantaneous positive current flowing into the dc bus, as shown in Fig. 6.1, is a function of the current through the diodes and IGBTs of either the top or bottom three switches where

$$\begin{aligned} i_{dc} &= (i_{d1} + i_{d3} + i_{d5}) - (i_{s1} + i_{s3} + i_{s5}) \\ &= -(i_{d2} + i_{d4} + i_{d6}) + (i_{s2} + i_{s4} + i_{s6}). \end{aligned} \tag{6.9}$$

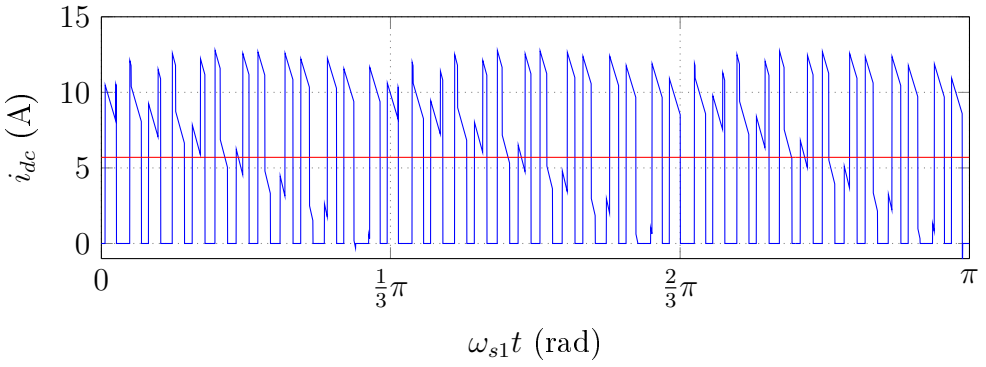

Figure 6.5: Instantaneous and average dc bus current.

Figure. 6.5 shows the instantaneous dc bus current in blue and the average dc bus current I_{dc} in red. The dc bus voltage is regulated to a constant 355 V and the dc bus capacitors labelled C in Fig. 6.1 remain charged, hence the current flowing into the capacitors (at equilibrium) has a mean value of 0 A (only the ripple component of the instantaneous dc bus current will flow into the capacitors). At the maximum average dc bus current of 5.7 A, the rms value of the ripple component was calculated in MATLAB as 5.07 A. The maximum combined rms current the capacitance C is rated to is 9.7 A as stated in the dc bus capacitance design of Section 3.1.2. The maximum combined rms ripple component of the dc bus current from both the converter and inverter circuit, at equilibrium, equals 9.61 A and is thus within the allowed operating range of the capacitors.

6.1.1 Generator Voltage and Current

The inverter phase voltages v_u, v_v and v_w, shown in Fig. 6.1, are applied to the respective generator stator terminals. The induction generator is however connected in delta configuration, thus the line-to-line voltages applied across each of the three generator phases, as shown in Fig. 6.1, are given by

$$v_a = v_u - v_v, \tag{6.10}$$

$$v_b = v_v - v_w, \tag{6.11}$$

and

$$v_c = v_w - v_u. \tag{6.12}$$

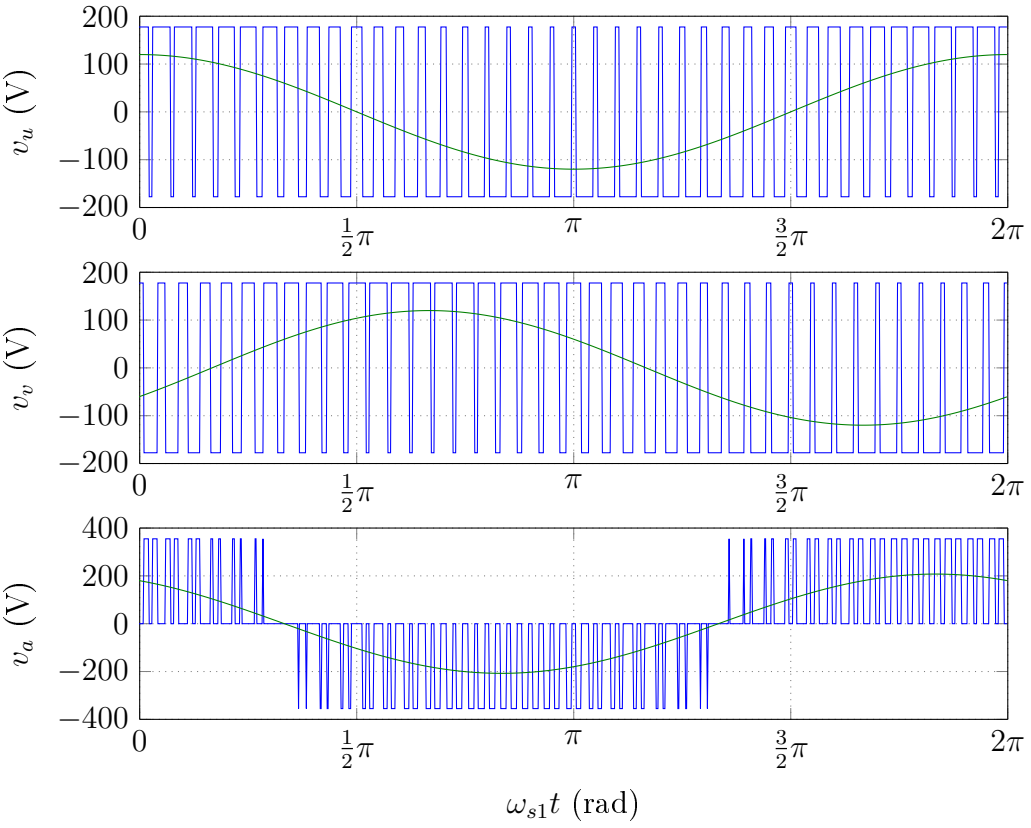

Figure 6.6: Instantaneous and fundamental line and phase voltages.

The two inverter phase voltages v_u and v_v are shown in Fig. 6.6 in blue, along with the resulting line voltage v_a. The fundamental component of each waveform is also indicated in green. The applied line voltages cause induced line currents to flow and are calculated using

$$\boldsymbol{I_{LL}} = \frac{\boldsymbol{V_{LL}}}{Z_{eq}}, \tag{6.13}$$

where $\boldsymbol{I_{LL}}$ and $\boldsymbol{V_{LL}}$ denote the respective phasor line currents and voltages of the generator as shown in Fig. 6.1. The equivalent generator impedance Z_{eq} is given in (6.6). The amplitudes of the line currents, and thus also the amplitudes of the inverter phase currents, will remain fairly constant with a change in angular frequency since both voltage and impedance change with respect to frequency. However, at low angular frequencies the relationship does not hold and current is seen to decrease with frequency and voltage.

The generator inductance as seen at the stator terminals is approximated as the sum of the two leakage inductances, L_{ls} and L_{lr}. The approximation is valid since the magnetising inductance L_m, connected in parallel with the rotor leakage inductance L_{lr}, is 20 times larger than the rotor leakage inductance and will thus have a negligible effect on the total generator inductance as seen from the stator terminals. The approximate generator inductance L_g is thus calculated from the machine parameters, derived in Chapter 5, as

$$L_g = \frac{X_{ls} + X_{ls}}{\omega_{s0}} = \frac{6.6}{2\pi 50} = 21 \text{ mH}, \tag{6.14}$$

where ω_{s0} is the rated angular generator velocity. The inductance is seen to be very large. Since current is equal to the time integral of the applied voltage divided by the inductance, the generator will produce a sinusoidal phase current with a small ripple component as shown in Fig 6.7. From simulation, the maximum current ripple is observed to occur when the duty cycle is 50 %, and has a peak-to-peak value of 0.155 A at a switching frequency of 20 kHz.

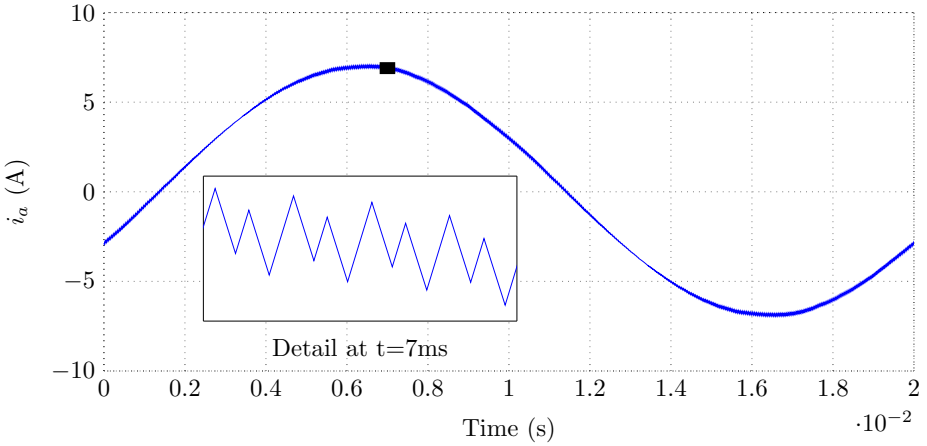

Figure 6.7: Instantaneous line current.

From the line currents the equivalent inverter phase currents shown in Fig. 6.1 are calculated as

$$i_u = i_c - i_a, \tag{6.15}$$

$$i_v = i_a - i_b, \tag{6.16}$$

and

$$i_w = i_b - i_c. \tag{6.17}$$

The amplitudes of the fundamental phase currents are $\sqrt{3}$ times larger than that of the fundamental line currents and lags the line currents by 30 degrees. The inverter phase current ripple will thus also increase by $\sqrt{3}$ to a peak-to-peak value of 0.22 A. The currents through the switches and diodes do in fact have a small ripple component, but this is negligible for the purpose of loss calculations.

6.1.2 IGBT Power Loss and Heat Sink Design

The IGBT module used is the FS30R06W1E3 module from Infineon. Table 6.1 shows the characteristic values of the chosen IGBT module.

Table 6.1: FS30R06W1E3 IGBT module parameter values.

Parameter	Description	Value
V_{CES}	Maximum collector-emitter voltage	600 V
I_{Cnom}	Maximum continuous dc collector current	30 A
I_{CRM}	Maximum repetitive peak collector current	60 A
V_{GES}	Maximum gate-emitter peak voltage	±20 V
$V_{CE(on)}$	Collector-emitter saturation voltage	1.25 V
t_{on}	Turn-on (rise) time	28 ns
t_{off}	Turn-off (fall) time	165 ns
$R_{\theta jc}$	Thermal resistance, junction to case	0.9°C/W
$R_{\theta cs}$	Thermal resistance, case to sink	0.85°C/W
V_F	Forward diode voltage	1.23 V

The inverter phase currents i_u, i_v and i_w are of sinusoidal form with a ripple component superimposed on them as described previously. For loss calculations the approximation is made that these currents are pure sinusoids. The phase currents are out of phase with the fundamental frequency of the phase voltages v_u, v_v and v_w as explained. The time period for one complete current or voltage sine wave is denoted T_1.

Similarly as with the MOSFET power losses, the IGBTs also have conduction, switching and diode losses. A sinusoidal current is positive and negative for the same duration of time; hence the switching losses in all six switches are identical. The losses are calculated for switch S_1. The currents through the IGBT and diode of S_1 are seen in Fig. 6.4. As described before, during the positive half-cycle of the fundamental phase current i_{uf}, most of the current will flow from the generator towards the dc bus through the forward biased diode D_1. Alternatively, current will flow through the IGBT of S_2 when it is on. During the negative half-cycle of i_{uf} while S_1 is on, current will flow through the IGBT of S_1, otherwise current will flow through the diode D_2.

First consider the conduction losses. In order for an IGBT to conduct current it needs an on-voltage across the collector and emitter terminals referred to as $V_{ce(on)}$ or V_{on}. The average power dissipated in the IGBT of switch S_1 over a single period T_1 is given by [11]

$$P_{cond} = V_{on} I_{s1}, \tag{6.18}$$

where I_{s1} is the average current through the IGBT of S_1. The average current is calculated from the fundamental phase current through S_1 as well as the duty cycle of switch S_1. The fundamental phase current i_{uf} is defined in (6.7) and repeated here for convenience:

$$i_{uf} = I_p \cos(\omega_{s1} t + \phi) = I_p \cos(\theta + \phi), \tag{6.19}$$

where I_p is the amplitude of the fundamental phase current and ω_{s1} is the angular frequency of each of the modulator reference voltages. The angle ϕ denotes the phase angle and was calculated in (6.6) as 36.38°. Both the amplitude of the fundamental phase current I_p and the phase angle ϕ will remain fairly constant with respect to the angular frequency, except at low angular frequencies, where the phase angle will increase (resulting in a decreased power factor) to a maximum of 180°, at which point the generator acts as a motor. Similarly the current amplitude I_p will decrease to 0 A due to the fundamental phase voltages decreasing with frequency. The loss calculations are performed for the worst case scenario, hence current I_p is at a maximum (15 A) and the phase angle is at 36.38°.

Figure 6.8 shows a detailed graph of the current through the IGBT of switch S_1 over three switching periods. During the on-time of each switching period T_s, the current i_{s1} is assumed constant as shown in red in Fig. 6.8, but the amplitude at each switching period will vary [31]. By using a Riemann sum approximation the area of the waveform shown in Fig. 6.8 can be calculated. When divided by the time period T_1, this results in the average current I_{s1} such that

$$I_{s1} \approx \frac{1}{T_1} \sum_{i=1}^{N} d_1 I_p \cos(\omega_{s1} t_i + \phi) T_s, \tag{6.20}$$

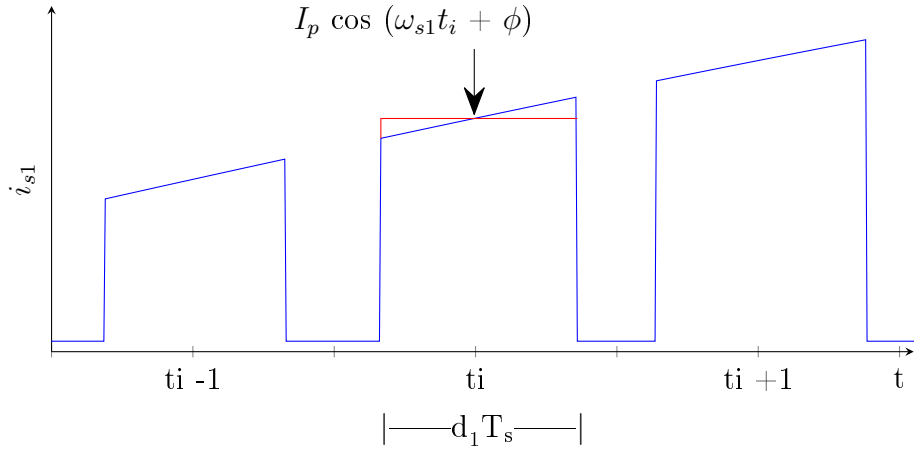

Figure 6.8: Average switching current approximation taken from [31].

where the duty cycle d_1 of switch S_1 is given in (6.8). By expanding (6.20) into integral form and also substituting $\omega_{s1}t$ for the angle θ, the average current over one angular rotation of 2π can be calculated. The lower and upper limits of the integral are derived from Fig. 6.4 which shows current only flows through the IGBT of S_1 when $\omega_{s1}t$ is between $\frac{\pi}{2} - \phi$ and $\frac{3\pi}{2} - \phi$ radians. With positive current defined as flowing into the dc bus, the average current I_{s1} is calculated as

$$\begin{aligned} I_{s1} &= -\frac{1}{2\pi} \int_{\frac{\pi}{2}-\phi}^{\frac{3\pi}{2}-\phi} \frac{1}{2} \left[1 + m_a \cos(\theta)\right] I_p \cos(\theta + \phi) d\theta \\ &= -\frac{I_p}{4\pi} \int_{\frac{\pi}{2}-\phi}^{\frac{3\pi}{2}-\phi} \left[\cos(\theta + \phi) + m_a \cos(\theta)\cos(\theta + \phi)\right] d\theta \\ &= -\frac{I_p}{4\pi} \int_{\frac{\pi}{2}-\phi}^{\frac{3\pi}{2}-\phi} \left[\cos(\theta + \phi) + \frac{m_a}{2}\cos(2\theta + \phi) + \frac{m_a}{2}\cos(-\phi)\right] d\theta \\ &= \frac{I_p}{2\pi} - \frac{I_p m_a}{8}\cos(\phi) \\ &= 1.13 \text{ A}. \end{aligned} \tag{6.21}$$

The modulation index m_a is defined in (6.3). The maximum rated machine current of 15 A was used for I_p. From (6.18) and with V_{on} given as 1.25 V in Table 6.1, the average conduction losses for switch S_1 was calculated as 1.41 W.

The switching losses are due to the small amount of time during which there is current through as well as voltage across the IGBT when it changes state, either from on to off or from off to on. These time periods are defined as t_{on} and t_{off} respectively. With reference to Fig. 6.4, the switching losses in the IGBT of S_1 during one angular rotation w_{s1} are approximated by [31]

$$\begin{aligned} P_{switch} &\approx \frac{1}{T_1}\sum_{i=1}^{N}\frac{1}{2}V_{dc(pp)}I_p\cos(\omega_{s1}t_i+\phi)(t_{on}+t_{off}) \\ &= \frac{V_{dc(pp)}I_p}{2T_1T_s}(t_{on}+t_{off})\sum_{i=1}^{N}\cos(\omega_{s1}t_i+\phi)T_s \\ &\approx \frac{V_{dc(pp)}I_p}{4\pi T_s}(t_{on}+t_{off})\left[-\int_{\frac{\pi}{2}-\phi}^{\frac{3\pi}{2}-\phi}\cos(\theta+\phi)d\theta\right] \\ &= \frac{V_{dc(pp)}I_p}{2\pi T_s}(t_{on}+t_{off}) \\ &= 3.27 \text{ W}, \end{aligned} \tag{6.22}$$

where the peak-to-peak dc bus voltage $V_{dc(pp)}$ is 355 V and the switching frequency f_s is 20 kHz.

When switch S_1 is off and the fundamental phase current i_{uf} is negative, current will flow through the diode of S_2. With reference to Fig. 6.4 and from (6.19) and (6.21), the average current I_{d2} is calculated during the negative half-cycle of i_{uf} as

$$\begin{aligned} I_{d2} &= -i_{uf} - I_{s1} \\ &= -\frac{1}{2\pi}\left[\int_{\frac{\pi}{2}-\phi}^{\frac{3\pi}{2}-\phi} I_s\cos(\theta+\phi)d\theta\right] - I_{s1} \\ &= \frac{I_s}{\pi} - I_{s1} \\ &= 3.64 \text{ A}. \end{aligned} \tag{6.23}$$

The average conduction loss through diode D_2 is given by

$$P_{D2} = V_F I_{d2} = 4.48 \text{ W}, \tag{6.24}$$

where V_F is the diode forward voltage given in Table 6.1 as 1.23 V. The total power loss through one diode and one IGBT during T_1 is thus

$$P_{tot} = P_{cond} + P_{switch} + P_{D2} = 9.16 \text{ W}. \tag{6.25}$$

The total power dissipated in each of the other diodes and IGBTs of the inverter is equal to the power dissipated in the IGBT of S_1 and the diode of S_2, respectively. The total power loss inside the complete IGBT module is thus given by

$$P_{mod} = 6P_{tot} = 54.96 \text{ W}. \tag{6.26}$$

The heat generated by the IGBT module due to the power loss P_{mod} is dissipated with the help of a heat sink. The rise in junction temperature due to the losses is given in (3.32) and repeated here for convenience:

$$\Delta T_j = P_T \left(R_{\theta jc} + R_{\theta cs} + R_{\theta sa} \right). \tag{6.27}$$

The junction temperature is permitted to rise to a maximum of 150°C. Absolute worst case ambient temperature is assumed to be 40°C, therefore ΔT_j = 110°C. From the IGBT module's datasheet the junction-to-case $R_{\theta jc}$ and case-to-sink $R_{\theta cs}$ thermal resistances are given as 0.9°C/W and 0.85°C/W respectively. From (6.26) and (6.27) the sink-to-ambient thermal resistance $R_{\theta sa}$ is required to be 0.251°C/W in order to keep ΔT_j below 110°C. A 150 mm by 210 mm MeccAL aluminium heat sink was available for this project. From the datasheet the sink-to-ambient thermal resistance is given as 0.15°C/W at an airflow rate of approximately 5 m/s. Airflow is provided by a small 12 V brushless dc fan mounted on the side of the heat sink. Thus

$$\Delta T_j = 54.96(0.9 + 0.85 + 0.15) = 104^\circ, \tag{6.28}$$

and the maximum allowed ambient temperature is thus 46°C. In the case of the chosen IGBT module the junction-to-ambient temperature is rather high. This is due to the junction-to-case and case-to-sink thermal resistances that are themselves high, due to the small size (and thus surface area) of the module.

6.1.3 Over-Temperature Protection

The IGBT module is equipped with a negative temperature coefficient (NTC) thermistor which can be used to detect over-temperature conditions. The temperature sensor is located on the case of the IGBT module. The circuit shown in Fig. 6.9 is used to detect the temperature of the IGBT module. A voltage divider circuit is used to obtain a voltage corresponding to the resistance of the thermistor, which is a function of the IGBT module's temperature.

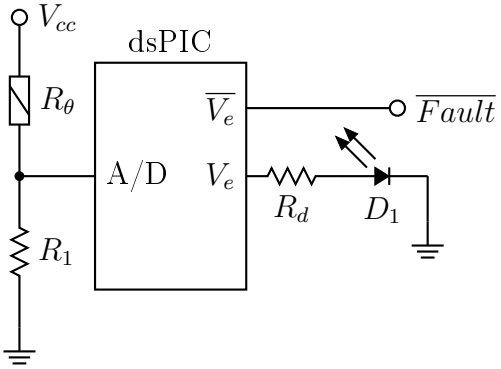

Figure 6.9: Temperature sensing circuit for the IGBT module.

At a case temperature of 100°C (equating to a junction temperature of 150°C), the thermistor R_θ has a value of 493 Ω with a deviation of ±5 % as indicated in

the IGBT module's datasheet. The recommended maximum power dissipation inside the NTC thermistor is $P_{max} = 9.6$ mW. The maximum current is thus

$$I_{max} = \sqrt{\frac{P_{max}}{R_{100}}} = 3.74 \text{ mA}. \tag{6.29}$$

The supply voltage V_{cc} for the circuit is chosen as 5 V and hence R_1 is calculated as

$$R_1 = \frac{V_{cc}}{I_{max}} - R_{100} = 843\ \Omega. \tag{6.30}$$

A 1 kΩ resistor was used for R_1. The voltage at the output of the voltage divider circuit is 3.35 V for an IGBT module temperature of 100°C. The output of the voltage divider is fed into one of the dsPIC's 12-bit analog-to-digital converter (ADC) inputs. The dsPIC used as part of the inverter controller is thus also used to perform functions related to the protection of the inverter circuit and general housekeeping tasks.

The dsPIC is programmed to produce an ADC interrupt every 0.8 ms. Inside the interrupt subroutine the ADC's value is compared with the decimal value of 2744 which corresponds to 3.35 V. If the ADC's value is smaller than 2744, the interrupt is cleared and the dsPIC continues to function normally.

If however the value is bigger than 2744, a 5 V error signal V_e is produced at one of the dsPIC's digital outputs and a red LED is turned on indicating an over-temperature condition occurred. Also, one of the dsPIC's digital output lines referred to as the $\overline{Fault}$ line, is set low (0 V). The resistor R_d shown in Fig. 6.9 has a value of 220 Ω and is used to limit the current through diode D_1 to less than 15 mA.

The six PWM signals (one for each IGBT) generated by the inverter control circuitry each pass through a high-speed CMOS logic 2-input CD74HC08 AND gate before feeding into an optocoupler located inside a gate driver IC. The other input to the respective AND gates is an error signal generated by the dsPIC $\overline{Fault}$ line. A block diagram of this circuit for one PWM channel is shown in Fig. 6.10.

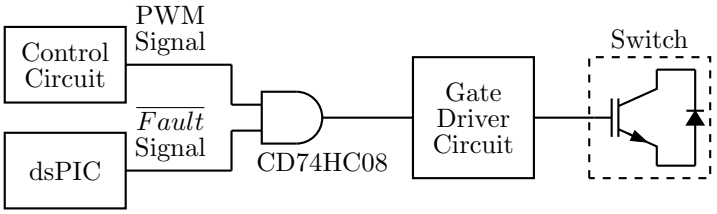

Figure 6.10: PWM signal and error signal integration.

Take for example switch S_1. The controller generates a desired PWM switching signal for S_1. This PWM signal, along with the error signal, is passed through

the two input AND gate. The output of the AND gate feeds the gate-drive circuit used to turn switch S_1 on and off. If the error signal is low, meaning a fault condition exists, then the output of the AND gate will remain low. Hence, the signal that is sent to the gate driver is also low, leaving switch S_1 in an off state. Consequently if the error signal is high, meaning there is no fault condition, the PWM signal is passed through the AND gate to the gate-drive circuit, enabling the desired controller switching action of S_1.

The same error signal is fed into all six AND gates, thus if a fault condition exists, all the switches are simultaneously switched off, setting the pole points of the inverter into a high impedance state.

Since a high junction temperature is caused by the switching action, with the switching action halted, the junction as well as case temperature will drop below the fault threshold temperature. The LED powered by the dsPIC will however not turn off if the case temperature drops below 100°C, nor will the inverter start switching again. The dsPIC $\overline{Fault}$ line will remain low. The dsPIC and controller circuity have to be restarted in order to clear the error condition and resume normal switching action at the IGBT gates. This is done purely for safety purposes and to ensure the cause of the fault condition is dealt with.

To validate this safety feature a heatgun was used to heat the bottom of the IGBT module casing (which is usually connected to the heat sink) to above 100°C. The red LED was observed to turn on and the inverter switching action terminated. Only once the circuit was restarted did the LED turn off and the inverter resume its switching action. The temperature at which this safety feature responded was measured by an infrared thermometer as roughly 100°C.

6.1.4 Isolated Gate-Drive Circuitry

The isolated gate-drive circuit used to communicate the switching signals to the gate of each IGBT is similar to the gate-drive circuit used for the MOSFET switches described in Section 3.1.5. To provide isolation between the control circuit and switches an IGBT gate-drive optocoupler IC is used. The gate driver is powered by a small push-pull oscillator circuit with a toroidal transformer and two fast rectifier diodes, identical to the circuit used in Section 3.1.5. The supply voltage to the oscillator circuit is however changed to 15 V and the transformer ratio to 10:11. The gate driver IC supply voltage is thus 16.5 V.

The gate driver IC chosen is the ACPL-333J gate driver from Avago Technologies. It is specifically designed as an IGBT gate-drive optocoupler equipped with integrated (V_{ce}) desaturation detection and feedback, undervoltage lockout and active Miller clamping [35]. The characteristic values of the gate driver are given in Table 6.2.

Table 6.2: ACPL-333J gate driver characteristic values.

Parameter	Description	Value
V_{CC2}	Positive supply voltage range	15-30 V
I_O	Maximum peak output current	2.5 A
V_{IORM}	Maximum working insulation voltage	1414 V
V_{UVLO}	Undervoltage lockout threshold	11.6 V
V_{DESAT}	Desaturation detection threshold	7 V
I_M	Maximum active Miller clamp current	1.7 A
t_p	Maximum propagation delay time	250 ns
CM	Common mode transient immunity	50 kV/μs

The maximum voltage across one of the IGBT switches is the rail-to-rail bus voltage of 355 V. The turn-on time of the switches is given as 28 ns and the turn-off time as 165 ns in Table 6.1. The turn-on time is significantly faster than the turn-off time; hence the maximum rate of change of IGBT voltage occurs when the switch is turned on where

$$\frac{dV}{dt} = \frac{V_{max}}{t_{on}} = 12.7 \text{ kV}/\mu\text{s}. \tag{6.31}$$

The dV/dt rating of the gate driver is thus sufficient to support the switching action of the IGBTs, since the gate driver is rated to withstand 50 kV/μs.

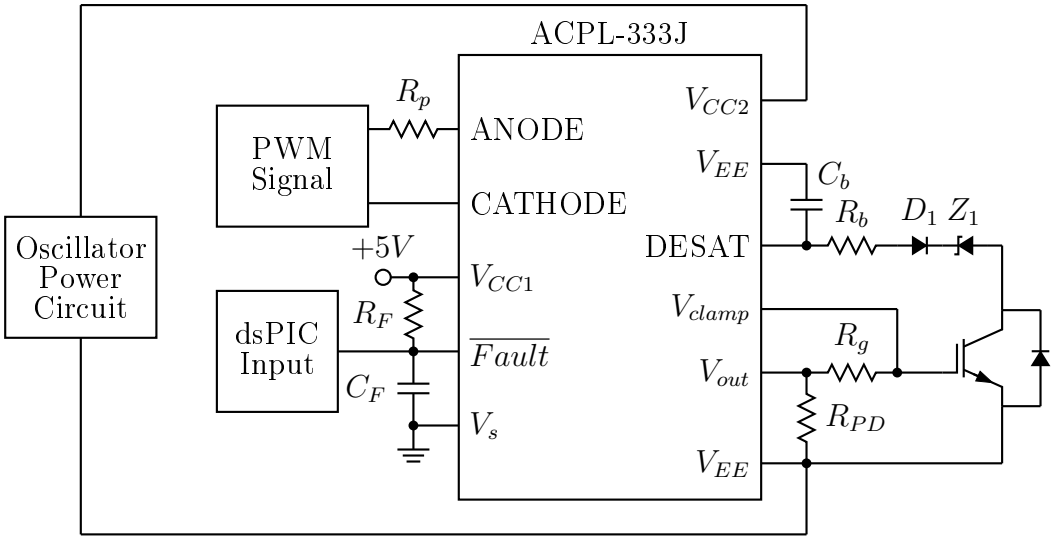

Figure 6.11: Block diagram of the IGBT gate-drive circuit.

A block diagram of the isolated gate-drive circuit is shown in Fig. 6.11. During normal operation the PWM signal from the control circuit is fed through

resistor R_p into the anode of the light emitting diode located inside the gate driver's optocoupler which then controls the output voltage V_{out} (as either high or low). The resistor R_p is chosen as 470 Ω. At the same time the desaturation detection circuitry is continuously monitored and the $\overline{Fault}$ line output voltage is high.

Once the desaturation detection picks up a V_{ce} value of more than 7 V it triggers a fault condition, during which time the output voltage V_{out} is reduced to zero. This allows the switch to be turned off softly and prevent large di/dt induced voltage spikes. The internal fault feedback is activated which changes the $\overline{Fault}$ line voltage from high to low in order to notify the control circuit. The PWM signal from the control circuit is ignored during the fault period. After a fixed period of approximately 26 μs the fault pin is reset and normal operation will continue unless V_{ce} is still larger than 7 V.

The fault feedback is given as a digital input to the dsPIC digital signal processor. Similarly as with an over-temperature fault, a yellow LED is switched on indicating an overcurrent fault occurred at one or more of the IGBT switches. The dsPIC output $\overline{Fault}$ line is set low and the same sequence of events will follow as described in the previous subsection. Essentially all switching action is stopped and the inverter is shut down. Again the circuit is required to restart before the dsPIC $\overline{Fault}$ line will change to a high state, allowing the switching action to resume and for the yellow LED to turn off.

The output of the gate driver is controlled by the PWM control signal, the protection circuitry, the desaturation detection circuitry as well as by the undervoltage lockout protection. If the voltage supplied by the oscillator circuit to the gate driver is less than 11.6 V, V_{out} is not allowed to go high due to the undervoltage lockout feature of the gate driver. Once the supply voltage is again greater than the threshold voltage, the output is allowed to go high. This feature protects the gate driver and the switch if the oscillator circuit were to fail.

The active Miller clamp capability allows the use of a positive supply voltage only for the gate driver, while still controlling the Miller current during high dV/dt transients. When the IGBT is switched off the gate voltage is monitored. The clamp circuitry is only activated when the gate voltage drops below 2 V, providing a low impedance path to sink the Miller current quickly. The clamp is released as soon as the next optocoupler LED trigger from the control circuit is received.

To ensure the maximum output current the gate driver can supply is not exceeded, the gate resistor R_g shown in Fig.6.11 is required to have a minimum value of

$$R_{g(min)} = \frac{V_{cc2}}{I_O} = \frac{16.5}{2.5} = 6.6\ \Omega. \tag{6.32}$$

The final value for R_g was chosen as 10 Ω, thus limiting the output current to 1.65 A. To clamp the output voltage V_{out} at V_{cc2} (16.5 V) a pull-down resistor

is required and is recommended in the datasheet to sink 650 μA of current while the output is high. The pull-down resistor is calculated as $R_{PD} = \frac{16.5}{0.65}$ = 25.4 kΩ. The final value for the pull-down resistor was chosen as 27 kΩ.

The $\overline{Fault}$ output is connected internally within the gate driver to the collector of a BJT. A passive pull-up resistor R_F is thus required and the recommended value is given as 2.1 kΩ. A 2.2 kΩ resistor was used for R_F. Along with the pull-up resistor, a 1 nF filtering capacitor C_F is recommended between $\overline{Fault}$ and V_s thus C_F was chosen as 1 nF.

As seen in Fig. 6.11 the desaturation detection circuit requires components R_b, C_b, D_1 and Z_1 to be connected externally from the gate driver to function correctly. The desaturation detection is internally set to trigger when V_{ce} equals 7 V, but for the chosen IGBT module this value is too high. At a V_{ce} value of approximately 1.7 V the collector current will already reach a value of around 25 A. Since the peak current through the inverter switches will never exceed 15 A, the desaturation protection is chosen to trigger at V_{ce} = 1.7 V. To achieve this a 3.9 V zener diode denoted by Z_1 in Fig. 6.11 was placed in series with D_1, a BYV26EGP ultrafast diode with a forward voltage of 1.4 V.

The values for R_b and C_b are specified in the datasheet as 100 Ω and 100 pF respectively. Resistor R_b is simply used as a protection resistor to limit the current from the gate driver such that it will not damage the IC. The desaturation fault detection circuitry is designed to stop any fault feedback once the IGBT switches on for a short period of time, to allow the V_{ce} value to fall below the threshold value. This time period can be adjusted by changing C_b. With C_b = 100 pF the blanking time is 2.7 μs.

6.1.5 Overvoltage Protection

The dc bus voltage is regulated by the dc-dc converter circuit. There are only two probable situations which will cause the dc bus voltage to exceed the nominal voltage of 355 V rail-to-rail. For both cases it is assumed there is no load connected to drain the bus voltage.

The bus voltage will rise if the current flowing from the generator into the dc bus is greater than the maximum current that each dc-dc converter is permitted to conduct. This occurs at a mean dc bus current of 6.857 A. The additional current will flow into the capacitors thus charging them to a value higher than the nominal voltage. A value of 6.857 A corresponds to an average inductor current of 10 A which is the current limit for charging the batteries as given in the battery datasheet. Since the mean bus current is regulated by the inverter circuit, it should never exceed an average current of 5.7 A unless the control circuit fails.

Secondly, the dc bus voltage will rise if the converter circuit is switched off while the generator is still supplying power to the dc bus. If the converter or batteries are disconnected there is nothing to sink the dc bus current except for the bus capacitors. They will continue to charge until they reach voltages

higher than what they are rated to operate at. In order to protect the capacitors as well as the other high voltage components such as the MOSFETs and IGBTs, overvoltage protection was added to the inverter control circuit.

The dc bus voltage is monitored and a scaled version of the bus voltage is fed into a comparator. If the bus voltage exceeds 365 V, which is 5 V higher than the allowed operating range, the comparator output changes from a high (5 V) to a low (0 V) state. The output of the comparator connects to one of the digital input lines on the dsPIC as well as directly to the AND gates used for sending the switching signals to the optocoupler inside the gate driver IC. The switching action is thus stopped immediately after the overvoltage fault occurred. The dsPIC ensures the fault is detected and keeps the digital output fault line low until the control circuit is reset.

6.2 PWM Controller Design

A block diagram of the proposed PWM control circuit is shown in Fig. 6.12. A double control loop approach is followed with an inner and outer control loop. The inner loop functions to control the amount of current flowing from the inverter into the dc bus, while the outer control loop regulates the battery voltage of the converter. The inner current control loop measures and compares the mean dc bus current with the set-point voltage v_{seti} generated by the outer voltage control loop, where one volt at v_{seti} corresponds to 1.14 A of current supplied by the generator to the dc bus. The set-point v_{seti} is dependant upon the state of charge of the converter's batteries as determined by the voltage control loop.

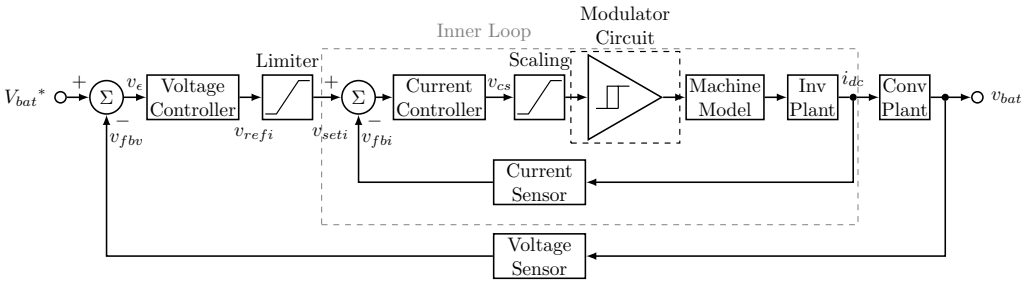

Figure 6.12: Block diagram of the inverter control circuit.

The battery voltage set-point $V_{bat}{}^*$ is a constant corresponding to 272 V. The resulting individual battery potential is 13.6 V for each of the twenty lead-acid batteries connected to the converter circuit.

As seen from Fig. 6.12, the current set-point v_{seti}, generated by the voltage control loop, is limited to between 0 V and 5 V such that the average dc bus

current is limited to a minimum of 0 A (to ensure the induction machine never operates continuously as a motor) and a maximum of 5.7 A.

The magnitude of the control signal v_{cs} generated by the current controller, as seen in Fig. 6.12, is also limited to 5 V since it feeds into an analog input pin on the dsPIC DSP. The generator shaft speed is measured and also given as an input to the dsPIC. Inside the dsPIC the magnitude of the control signal is scaled according to the angular speed of the generator shaft to ensure a constant Volt/Hz ratio is maintained.

The dsPIC is responsible for producing the sinusoidal reference waveforms that are compared with the triangular carrier waveform to generate the required PWM switching signals for the six IGBTs. In Fig. 6.12 the PWM generation circuit is denoted as the modulator circuit and will be described in more detail in the subsections to follow.

Both the voltage and current controllers are designed using frequency domain analysis. The necessary time domain equations are derived to obtain the frequency domain equations by using the Laplace transform. The time domain simulations are only presented in the next chapter alongside the measured test results for comparison purposes.

6.2.1 Inverter Plant

The plant portion of the inverter circuit is shown in Fig. 6.13. It is used to identify the relationship between the generator line voltages and the current flowing into the dc bus. The inverter phase voltages, and hence also the generator line voltages, are controlled by the switching action of the IGBTs dictated by the current control loop.

The approximation is made that the instantaneous power flowing into the dc bus equals the instantaneous power flowing out of the generator, hence the switching and conduction losses are not taken into account. The dc bus current is related to either the inverter phase voltages and currents or the generator line voltages and currents, since the total instantaneous power from the inverter phase voltages and currents must equal the total instantaneous power from the generator line voltages and currents. With reference to Fig. 6.13 the instantaneous power flowing into the dc bus is given by [11]

$$V_{dc(pp)} i_{dc} = v_a i_a + v_b i_b + v_c i_c, \tag{6.33}$$

where $V_{dc(pp)}$ is the converter regulated dc bus voltage of 355 V and i_{dc} is the time-varying dc bus current. The line currents are sinusoidal with a small ripple component superimposed on them and can thus be viewed as pure sinusoids with only the fundamental components present.

The triangular carrier waveform's switching frequency is much larger than the fundamental frequency of the line voltages, resulting in a large frequency modulation ratio. The amplitudes of the subharmonics will thus be very small

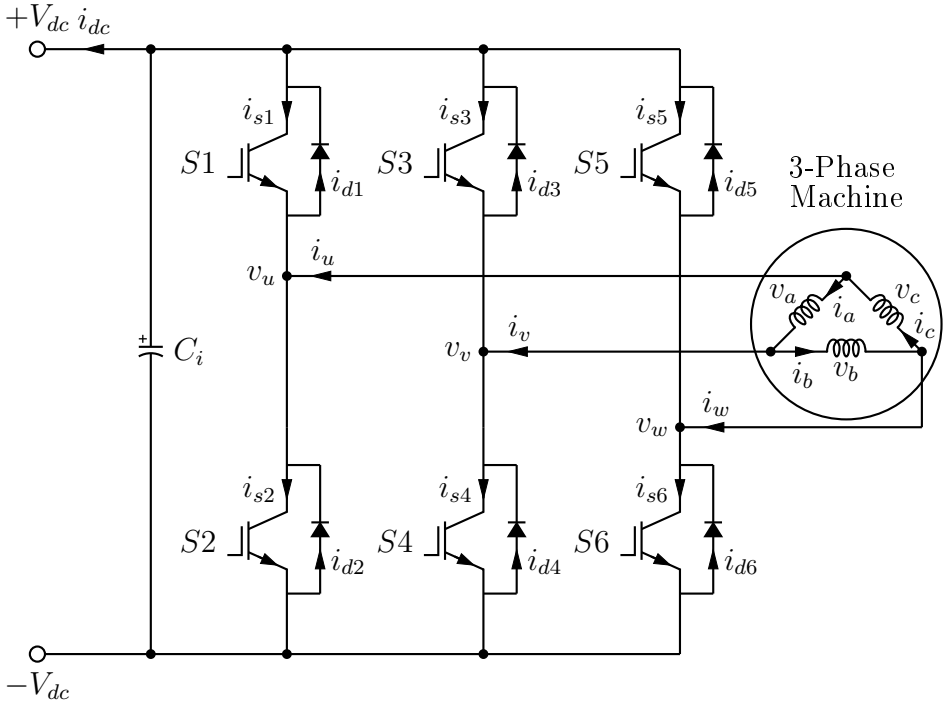

Figure 6.13: Bidirectional inverter circuit.

and it can be approximated that only the fundamental frequency component of the line voltages will contribute towards the instantaneous power generated by the induction machine [11]. With the line voltages and currents approximated as fundamental line voltages and currents, (6.33) reduces to

$$\begin{aligned} i_{dc} &= \frac{2V_{s(rms)}I_{s(rms)}}{V_{dc(pp)}} [\cos(\omega_{s1}t)\cos(\omega_{s1}t+\phi) \\ &\quad + \cos(\omega_{s1}t-120°)\cos(\omega_{s1}t-120°+\phi) \\ &\quad + \cos(\omega_{s1}t+120°)\cos(\omega_{s1}t+120°+\phi)] \\ &= \frac{3V_{s(rms)}I_{s(rms)}}{V_{dc(pp)}}\cos\phi, \end{aligned} \tag{6.34}$$

where $V_{s(rms)}$ and $I_{s(rms)}$ are the rms values of the fundamental line voltages and currents, respectively. The angle ϕ denotes the power factor angle as described earlier. The rms values of the generator line voltages and currents are related by the equivalent generator impedance Z_{eq} such that

$$I_{s(rms)} = \frac{V_{s(rms)}}{|Z_{eq}|}, \tag{6.35}$$

where $|Z_{eq}|$ is the magnitude of the equivalent generator impedance given in (5.17). Recall the amplitudes, and therefore also the rms values of the fundamental line voltages, are varied in proportion to the angular frequency of

the fundamental waveforms in order to maintain constant rms flux within the generator core. The impedance Z_{eq} is also frequency dependant and thus from (6.35) the rms value of the line currents will remain fairly constant. At low frequencies (below 20 Hz) the real component of the impedance dominates the imaginary component that varies with frequency and hence $I_{s(rms)}$ will change with $V_{s(rms)}$.

The control circuit is designed for the worst case scenario and thus $I_{s(rms)}$ is assumed constant and equal to the maximum delta connected rms current given in the machine datasheet as 6.07 A for the frequency domain analysis.

The phase angle ϕ with respect to the generator frequency is shown in Fig. 6.14 and was calculated using the equivalent generator model derived in Chapter 5. The phase angle is seen to remain fairly constant at frequencies above 25 Hz. The generator will only be allowed to operate at frequencies above 7 Hz since it draws instead of delivers current at lower frequencies. The angle ϕ is assumed constant and equal to 36.38° as calculated from (6.6) for the frequency domain analysis.

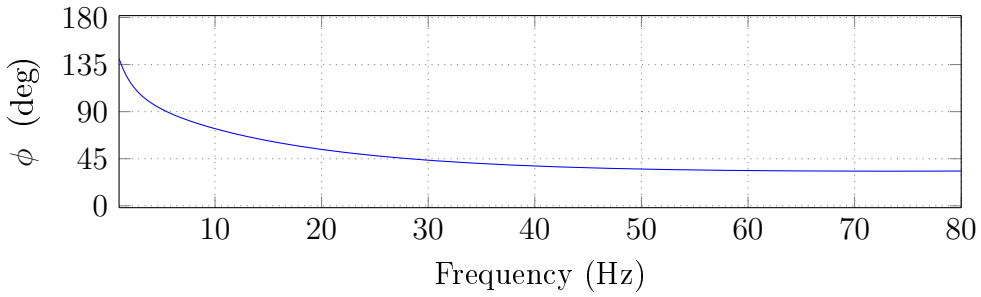

Figure 6.14: Phase angle over generator operating frequency range.

The Laplace transform of the (6.34) yields

$$I_{dc}(s) = \frac{3I_{s(rms)}}{V_{dc(pp)}} \cos\phi V_s(s), \tag{6.36}$$

where $V_s(s)$ is the rms line voltage of the generator that varies with frequency. The transfer function of the inverter plant $G_p(s)$, describing the average dc bus current as a function of the rms line voltage, is thus given by

$$G_p(s) = \frac{I_{dc}(s)}{V_s(s)} = \frac{3I_{s(rms)}}{V_{dc(pp)}} \cos\phi. \tag{6.37}$$

The plant portion of the inverter is thus combined with the machine model shown in Fig. 6.12.

6.2.2 Digital Signal Processor Interfacing

The main function of the dsPIC is to assist with the control of the inverter switches. It is also used alongside protection circuitry as mentioned throughout this chapter. The 30F4013 dsPIC from Microchip was chosen for its DSP capabilities and functionality. The parameters of the dsPIC is summarised in Table. 6.3.

Table 6.3: Parameter values of the dsPIC30F4013 DSP.

Parameter	Value
Architecture	16-bit
CPU speed	30 MIPS
Program memory	48 KB
RAM	2048 B
EEPROM	1024 B
Operating voltage	2.5 V to 5.5 V
Operating temperature	-40°C to 125°C
Pin count	40
Input/output pins	30
Communication peripherals	2 UART, 1 SPI, 1 I2C
Analog peripherals	1-ADC, 13 x 12-bit at 200 ksps
Timers	5 x 16-bit, 2 x 32-bit

The dsPIC is operated at 5 V and 10 MHz. An external 10 MHz crystal oscillator was used to generate the internal 10 MHz clock. The dsPIC was programmed using a dsPICDEM 2 development board and an MPLAB ICD2 in-circuit debugger.

The generator is driven by an identical induction motor controlled by a commercial off-the-shelf variable-speed drive system to simulate airflow through a turbine that would otherwise apply torque to the generator shaft. Due to the large moment of inertia, the speed at which the generator shaft is turning will not change rapidly; hence vector control is not required. The stator voltages are controlled as a function of the dc bus current, but Volt/Hertz control is also included inside the inner control loop using the dsPIC to ensure the machine's magnetic rms flux stays constant. The detailed operation of the dsPIC is described in this section.

The current controller produces a control signal v_{cs} which feeds into one of the 12-bit ADC channels on the dsPIC. The dsPIC is operated at 5 V, hence the maximum allowed voltage at any of the input pins is also 5 V. The control signal v_{cs} is limited to between 0 V and 5 V by means of an active clamp circuit identical to the circuit used for limiting current and voltage inside the converter as described in Section 3.2.4.

To determine the shaft speed of the generator a magnetic pick-up sensor was used. The functioning of the magnetic pick-up circuit is demonstrated in Fig. 6.15. The magnetic pick-up consists of a small permanent magnet and a coil wound around the magnet. The permanent magnet establishes a magnetic field that couples to the coil. When a ferromagnetic material passes in close proximity to the magnet, the magnetic field is displaced about the coil. Thus, by Faraday's law, a voltage is induced in the winding. The output voltage is proportional to the strength and rate of change of the magnetic field coupled to the winding.

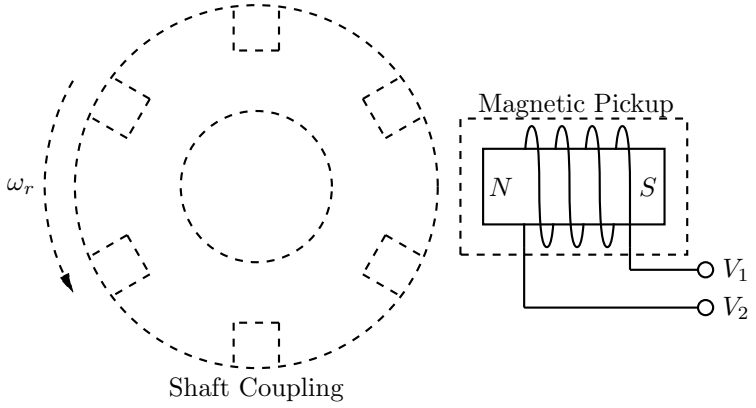

Figure 6.15: Shaft coupling with magnetic pick-up for speed feedback.

The shaft coupling, connecting the generator and motor shafts, was used as the ferromagnetic object, as shown in Fig 6.15. Six holes with a diameter of 14 mm each, separated exactly 60° from each other, were drilled 10 mm deep into the circular shaft coupling. The magnetic pick-up was mounted approximately 2 mm away from the shaft. One complete rotation thus produces 6 voltage pulses between the two output terminals V_1 and V_2.

The output signal of the magnetic pick-up is processed using the circuit shown in Fig. 6.16. The coil wound around the permanent magnet can be represented as an inductor L in series with a resistor R. The output voltage pulses are first passed through an operational amplifier with a gain of approximately 3 to amplify the speed feedback signal. Once the output of the op-amp exceeds 0.45 V, the LM311 comparator changes from a high (5 V) to a low (0 V) state. Even if the shaft is turning at very low speeds, the output voltage will exceed 0.45 V and thus generate a state-change at the comparator output. Positive feedback is added to provide hysteresis which ensures that no false state changes occur.

The output of the comparator is fed into one of the dedicated external interrupt pins on the dsPIC. The interrupt will trigger an interrupt subroutine

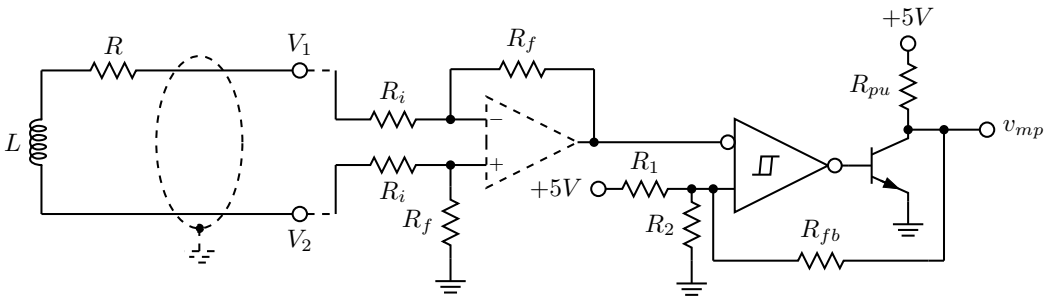

Figure 6.16: Magnetic pick-up interfacing with the dsPIC.

on every falling edge of the comparator output voltage v_{mp}. The values of the components used in Fig. 6.16 are given in Table 6.4

Table 6.4: Component values for the magnetic pick-up and dsPIC interfacing circuit.

Component	Value
L	350 mH
R	580 Ω
R_i	3.3 kΩ
R_f	10 kΩ
R_1	10 kΩ
R_2	1 kΩ
R_{fb}	22 kΩ
R_{pu}	1.8 kΩ

One of the dsPIC's two 32-bit timers is used to count the time interval between interrupts generated by the magnetic pick-up circuit. As soon as the first magnetic pick-up is received the timer is reset and starts counting from zero. One count is added every 100 ns since the timer is set to run at the internal 10 MHz clock speed of the processor. Once the second interrupt is received, the timer value is stored in memory and thereafter the timer is reset to once again start counting from zero. The value that is stored in memory is used to calculate the frequency of the generator shaft since

$$f = \frac{F_c}{6C_T}, \tag{6.38}$$

where f is the shaft frequency measured in Hertz, C_T is the timer value stored in memory and F_c is the clock frequency of 10 MHz. The factor $\frac{1}{6}$ is present due to the magnetic pick-up producing six interrupts during one complete shaft rotation. The measured shaft frequency f is further divided by a base frequency f_b of 65 Hz to generate a scaling factor K_c. A base frequency of

65 Hz was chosen to avoid saturation currents when the generator is operated at a slip of -5.47 %. The scaling factor scales the control signal v_{cs} to ensure the generator is always operated at constant flux, thus the maximum amplitude V_c of the dsPIC and DAC output modulator reference waveforms are calculated as

$$V_c = \frac{f}{f_b} v_{cs} = K_c v_{cs}. \tag{6.39}$$

If the measured frequency of the generator is less than 7 Hz, the control signal v_{cs} is gradually reduced to zero inside the dsPIC since the machine simulation predicted the generator is only able to supply power when operating at a frequency above 7 Hz. Below 7 Hz the generator will actually draw power from the dc bus to keep it running when operated at a slip of -5.47 %.

Similarly, the control signal v_{cs} is reduced to zero inside the dsPIC when the measured shaft frequency exceeds 75 Hz (4500 rpm), which is the specified maximum operating frequency of generator system. When the generator is running at either under 7 Hz or above 75 Hz an orange LED is switched on, visually indicating the generator shaft speed is out of range. When the control signal v_{cs} reaches zero the switches are all switching at a constant duty cycle of 50 % and the amplitudes of the fundamental phase voltages applied to the generator stator terminals are also zero. No power will thus be transferred between the generator and the dc bus.

The orange LED switch off once the shaft speed is again within the specified range. At the same time the control voltage is gradually increased to the desired value.

In order to generate the required PWM signals, three 120° separated sinusoids have to be compared with the 20 kHz triangular carrier waveform as explained in the previous section. The dsPIC is used to generate these three sinusoidal modulator reference waveforms using a look-up table (LUT) approach similar to the approach followed in [44] and [45] where a part of the sinusoid is pre-computed and stored in the memory of the processor used, thus forming a binary LUT.

The maximum resolution of the sine wave generated within the dsPIC is chosen as 12 bits, where the 12th bit is used to indicate the polarity of the sinusoid as either positive or negative. The sampling speed of the sine wave was chosen as 128 samples per 60°. The sine wave was modelled using MATLAB where the amplitude of the sine wave peaked at 2047 corresponding to the available 11-bit magnitude inside the dsPIC.

Since the induction generator is designed to function at a slip of -5.47 %, the number of samples during 60 degrees of rotation is $\frac{128}{0.948} = 135$ samples. To simplify the look-up process inside the dsPIC, the entire positive half of the sine wave generated in MATLAB was stored in the EEPROM. The EEPROM thus contain $135 \times 3 = 405$ samples where each sample is represented using 2 bytes.

The three sinusoidal modulator reference waveforms v_{ru}, v_{rv} and v_{rw} generated by the dsPIC, are shown in Fig. 6.17. Each have their own LUT pointer. The amplitudes of the modulator reference waveforms are equal and denoted V_c, as defined in (6.1) for v_{ru}. At a sample speed of 128 samples per every 60°, the counter value C_T is divided by 128 to produce a timer limit L_T for a 16-bit timer. Each time the 16-bit timer reaches the limit L_T an interrupt is generated and the three pointers are all incremented to point to the next corresponding value inside the LUT.

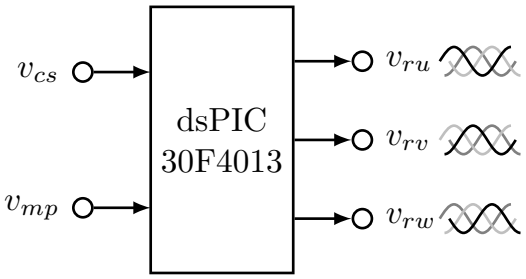

Figure 6.17: Three-phase reference waveform generation with the dsPIC.

The LUT value is then manipulated such that the 12th bit is set high if the sinusoid is negative. Also the scaling factor K_c is used to scale the magnitude of the LUT value (and thus also scale the magnitude of the sinusoid) according to the value read in by the ADC for v_{cs} and the speed of the generator shaft.

The dsPIC was programmed in assembly language using the MPLAB editor. Assembly was chosen instead of the C programming language to have precise control over the number of instruction cycles that occur after the magnetic pick-up produces an interrupt. This ensures the correct timer value is stored in memory and allows for a more accurate shaft speed calculation.

The three manipulated LUT values are communicated to a 12-bit AD7398 digital-to-analog converter (DAC) using the serial peripheral interface (SPI) protocol. The DAC outputs three modulator reference sinusoids, each with a maximum amplitude of 2.5 V and a dc offset of 2.5 V. The dc offset is removed and a gain of two is added using a differential LF353 operational amplifier. The three resulting modulator reference waveforms, with a maximum amplitude V_c of 5 V, are used for comparison with the triangular carrier waveform to generate the PWM switching signals using high-speed AD790JN comparators from Analog Devices.

The complete circuit diagram containing the dsPIC, DAC and magnetic pick-up interface circuit is given in Appendix A.2.2. A small PCB containing these circuit components is mounted on top of the analog control PCB. Both PCBs are given in Appendix B.2.2.

6.2.3 Current Control Loop

The current control loop, shown in Fig. 6.18, functions to control the mean dc bus current by controlling the switching action of the IGBTs using both analog and digital circuitry. Essentially the controlling of the switches allows the amount of power generated by the induction machine to be controlled, and since the dc bus voltage is assumed constant, the dc bus current is thus controlled. The digital part of the controller was already described in the previous subsection along with the PWM signal generation.

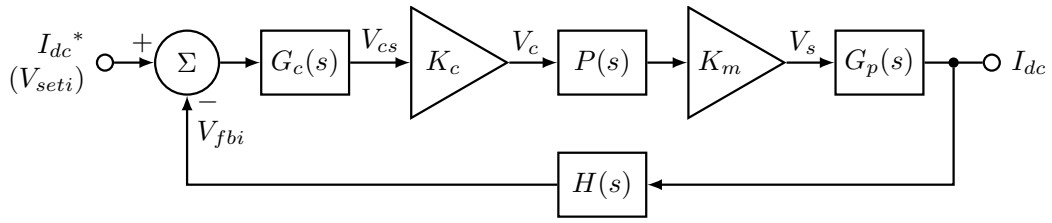

Figure 6.18: DC bus current control loop block diagram.

In Fig. 6.18 $G_p(s)$ denotes the transfer function of the inverter plant portion derived in (6.37) and the transfer function $H(s)$ denotes the current sensing feedback circuit. The current control loop's compensation amplifier is described by the transfer function $G_c(s)$.

The transfer function $P(s)$ shown in Fig. 6.18 is a third order Padé approximation [46] used to approximate the various time delays within the current control loop as a time-continuous function for frequency domain analysis. The time delays, mainly due to the dsPIC, can potentially cause system instability and it is therefore important to include the time delays in the frequency domain analysis. Note, a time delay introduces phase shift only and does not affect the magnitude of the control loop's response. The total control loop time delay was overestimated as 1 ms. The Padé function within MATLAB was used to model this time delay.

The scaling factor K_c used for the Volt/Hertz scaling within the dsPIC (as detailed in the previous subsection) is also included in the current control loop as shown in Fig. 6.18. The scaling factor has a maximum value of 1 and a minimum value of 0.11 (at a generator shaft frequency of 7 Hz). The gain denoted K_m in Fig. 6.18 is used to represent the modulator circuit and is described in detail next.

A linear model of the PWM circuit is assumed, thus a linear relationship exists between the sinusoidal modulator reference signals (v_{ru},v_{rv} and v_{rw}) and the fundamental inverter phase voltages (v_{uf},v_{vf} and v_{wf}). The rms voltage $V_{s(rms)}$ of the fundamental generator line voltages (v_{af},v_{bf} and v_{cf}) is related to the amplitude of the inverter phase voltages V_p by

$$V_{s(rms)} = \frac{\sqrt{3}}{\sqrt{2}} V_p. \tag{6.40}$$

Substituting (6.4) and (6.2) into the above equation yields

$$\begin{aligned} V_{s(rms)} &= \frac{\sqrt{3}}{2\sqrt{2}} m_a V_{dc(pp)} \\ &= \frac{\sqrt{3}}{2\sqrt{2}} \left(\frac{V_c}{V_r} \right) V_{dc(pp)} \\ &\approx \frac{0.612 V_{dc(pp)}}{V_r} V_c, \end{aligned} \tag{6.41}$$

where V_r is the amplitude of the triangular carrier waveform and V_c is dsPIC scaled amplitude of the modulator reference voltages. The Laplace transform of the above equation yields:

$$V_s(s) \approx \frac{0.612 V_{dc(pp)}}{V_r} V_c(s). \tag{6.42}$$

With reference to Fig. 6.18, the frequency dependant rms line voltage $V_s(s)$ and modulator reference waveform amplitude $V_c(s)$ are thus related by K_m where

$$K_m = \frac{V_s(s)}{V_c(s)} = \frac{0.612 V_{dc(pp)}}{V_r}. \tag{6.43}$$

The dc bus current is measured using an ACS756 fully integrated Hall effect sensor from Allegro. The characteristics of the sensor is summarised in Table 6.5.

Table 6.5: Allegro ACS756 Hall effect sensor characteristics.

Characteristic	Description	Value
V_{cc}	Supply voltage	5 V
I_{cc}	Supply current	10 mA
t_{PROP}	Propagation time	1 μs
I_p	Primary Sampled Current	$\pm$50 A
$Sens_{TA}$	Sensitivity	40 mV/A
E_{TOT}	Maximum total output error	$\pm$5 %
V_{ISO}	Voltage Isolation	3 kV
T_{OP}	Ambient Operating Temperature	-40°C to 125°C

At a sensitivity of 40 mV/A and a maximum dc bus current of 5.7 A, the maximum output voltage is 0.228 V. The desired output voltage is 5 V for the maximum dc bus current, hence a gain of 21.93 was required. The circuit used

to convert the measured current into the equivalent desired voltage is shown in Fig. 6.19. The component values for the current feedback circuit are given in Table 6.6.

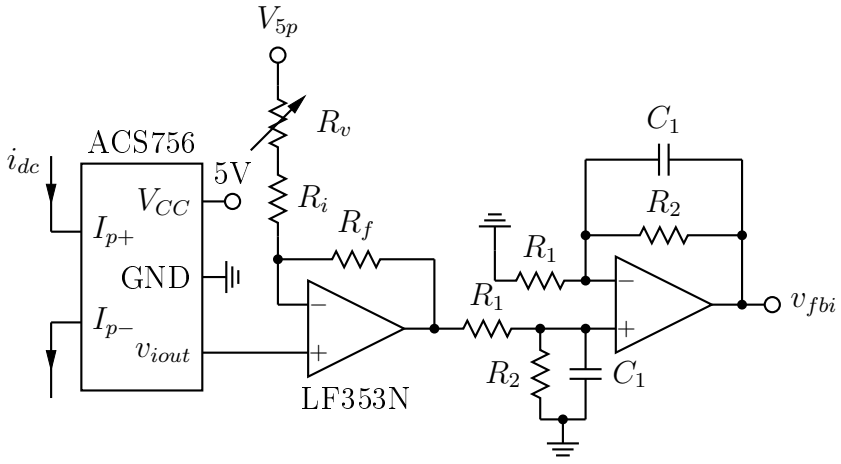

Figure 6.19: DC bus current sensor feedback circuit.

Table 6.6: Component values for the current feedback circuit.

Component	Value
V_{5p}	5 V
R_v	10 kΩ
R_i	4.7 kΩ
R_f	10 kΩ
R_1	3.3 kΩ
R_2	36.3 kΩ
C_1	100 nF

An LF353 operational amplifier is used to provide the additional gain required. The first op-amp circuit is used to remove the 2.5 V dc offset from the Hall effect sensor's output v_{iout}. The resistor R_v is a variable resistor to trim the dc offset in case of a small voltage offset error at the sensor's output for a 0 A measurement. The output voltage for the first op-amp circuit is given by

$$v_{out} = \frac{R_f}{R_i + R_v}(v_{iout} - V_{5p}) + v_{iout}. \tag{6.44}$$

The ratio between the feedback resistor R_f and the two input resistors $R_v + R_i$ should ideally equal one thus (6.45) becomes

$$v_{out} = 2v_{iout} - V_{5p}. \tag{6.45}$$

The input V_{5p} is a precision 5 V reference source generated by a REF02 IC from Analog Devices. With a dc offset of 2.5 V at v_{iout}, the output voltage v_{out} has a gain of 2 with respect to the two input voltages v_{iout} and V_{5p}.

The second op-amp circuit is a low pass filter with a transfer function of

$$L(s) = \frac{Z_f}{Z_i} = \frac{R_2}{R_1}\left(\frac{1}{1 + sC_1R_2}\right), \tag{6.46}$$

and a corner frequency of

$$f_1 = \frac{1}{2\pi C_1 R_2}, \tag{6.47}$$

which equals 43.84 Hz with the component values given in Table 6.6. The low pass filter is used to remove the ripple component from the measured dc bus current as well as provide a dc gain of 11. The transfer function for the complete current feedback circuit shown in Fig. 6.19 is denoted $H(s)$ and is given by

$$H(s) = \frac{V_{fbi}(s)}{I_{dc}(s)} = \frac{2R_{cs}R_2}{R_1\left(1 + sC_1R_2\right)}, \tag{6.48}$$

where R_{cs} equals 40 mΩ and is used to include the 40 mV/A sensitivity of the Hall effect sensor. With reference to Fig. 6.18 the open-loop transfer function of the current control loop $G_{ol}(s)$ is

$$G_{ol}(s) = G_c(s)K_cP(s)K_mG_p(s)H(s), \tag{6.49}$$

and closed-loop transfer function $G_{cl}(s)$ is

$$G_{cl}(s) = \frac{G_c(s)K_cP(s)K_mG_p(s)}{1 + G_c(s)K_cP(s)K_mG_p(s)H(s)}, \tag{6.50}$$

where $G_c(s)$ is the transfer function of the compensation amplifier and $G_p(s)$ is the transfer function of the inverter plant derived in (6.37). The frequency domain analysis of $G_{ol}(s)$ with the dsPIC scaling factor K_c at its maximum value of 1 is shown in Fig. 6.20, without the transfer function of the compensation amplifier present.

The magnitude plot shown in Fig. 6.20 has a corner frequency equal to f_1 and rolls off at -20 db/decade thereafter. The bandwidth of the current control loop without the compensation amplifier present is determined from Fig. 6.20 to be 37.3 Hz. The phase plot indicates a large phase shift mainly due to the third order Padé approximation of the time delay within the current control loop.

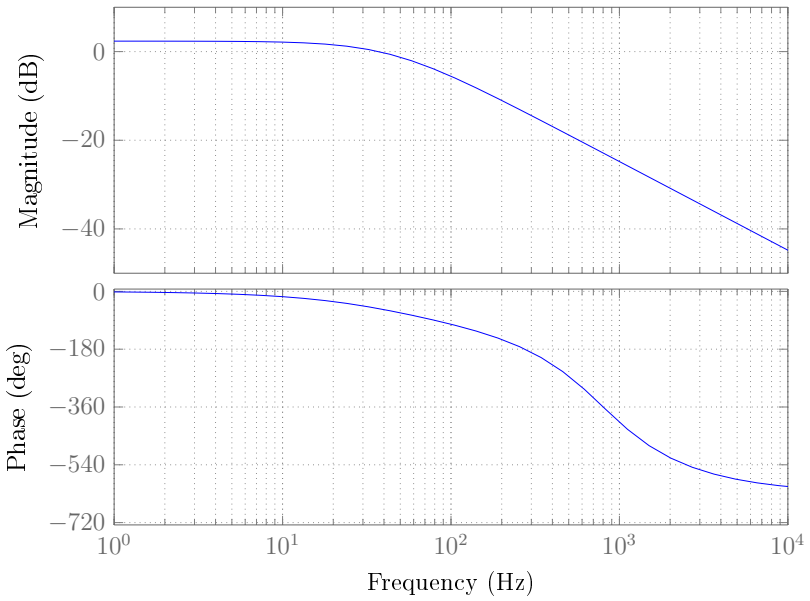

Figure 6.20: Bode plot of the open-loop response of the current control loop without the compensator present.

The speed of the current control loop should ideally be lower than the lowest operating speed of the generator (7 Hz) since the generator will inherently react slowly to a change in the applied stator voltages.

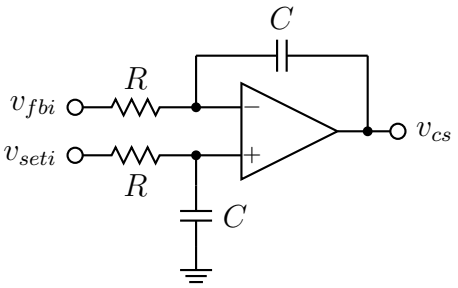

Figure 6.21: Active integrator compensation circuit.

In order to provide a theoretical infinite gain at dc, an integrator is required in the compensation amplifier. The integrator will also lower the bandwidth of the current control loop and is thus in itself an adequate compensation amplifier for the current control loop. The active integrator circuit is shown in Fig. 6.21. The transfer function for the compensation amplifier is given by

$$G_c(s) = \frac{V_{cs}}{V_{seti} - V_{fbi}} = \frac{1}{sCR}. \tag{6.51}$$

The resistor R was chosen as 120 kΩ and the capacitor C as 1 μF. The op-amp used is the LF353 JFET operational amplifier from STMicroelectronics.

The frequency domain analysis of both the open- and closed-loop transfer functions $G_{ol}(s)$ and $G_{cl}(s)$ are shown in Fig. 6.22. The open-loop transfer function is seen to have a unity gain crossover frequency of 1.74 Hz which is within the desired range. The corresponding phase margin is measured as 87.1° and the open-loop response shows a -20 db/decade roll-off when it crosses the zero dB line. The gain margin is determined from Fig. 6.22 as 39.6 dB. With both a positive gain and phase margin the current control loop is shown to be stable.

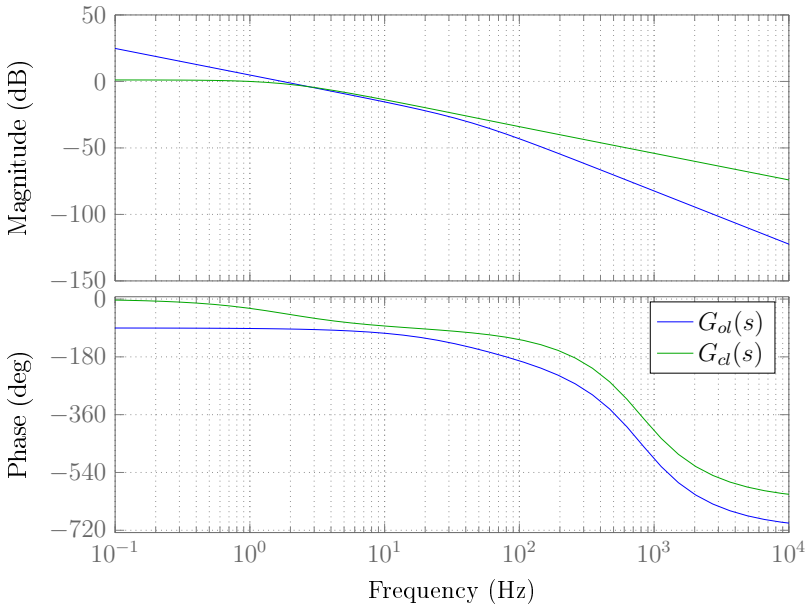

Figure 6.22: Bode plot of the open-loop response of the complete current control loop.

The closed-loop response shown in Fig. 6.22 has a dc gain of 1.135 dB corresponding to a loop sensitivity of 1.14 A of dc bus current per volt of excitation applied to the current set-point V_{seti}. At a maximum set-point voltage of 5 V the corresponding dc bus current will rise to and settle at 5.7 A as designed for.

Due to the large 1 μF capacitor used in the compensation amplifier, integral windup occurs. Recall the output of the compensator V_{cs} is limited to 5 V. The integral windup will cause a large initial current overshoot in the dc bus and will also lead to a slow settling time [47]. Since the current flowing into the batteries is current limited, a large current overshoot is undesirable, especially if it will take a prolonged period of time to settle. To combat the integral windup, a tracking back anti-windup scheme [41] is used. Figure 6.23 shows

a block diagram of the tracking back scheme when using an integrator for the compensation circuit.

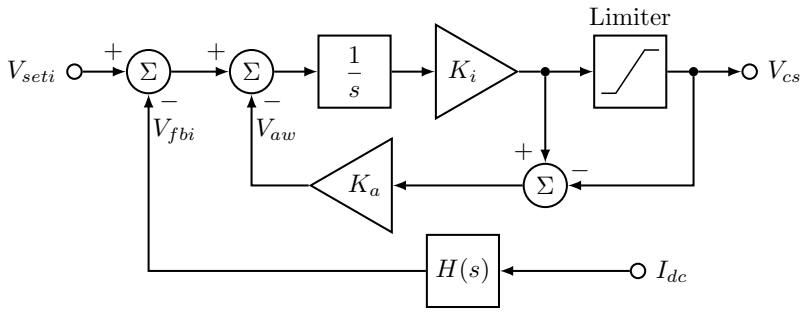

Figure 6.23: Tracking back anti-windup scheme with an integral controller.

The gain block labelled K_i in Fig. 6.23 is the integrating factor $\frac{1}{RC}$ from (6.51), while K_a is the anti-windup factor. The difference between the limited (saturated) output and the unsaturated output of the integrator is fed back to the input of the integrator after adding gain K_a to the signal, thus producing V_{aw}. Although it is desirable to make K_a very large to reduce the integrator windup quickly, it will also increase the settling time. Ideally the constant K_a should be close to unity when using an integral compensation method [41]. By testing the prototype circuit the optimal value for K_a was determined to be 1.27.

The anti-windup circuitry only affects the controller when the integrator output is higher or lower than the clamped output V_{cs}. When the integrator output is within the desired operating range, the saturated and unsaturated outputs are equal to each other and thus the difference between them is zero. The voltage at V_{aw} is thus also zero and will have no effect on the compensation circuit.

6.2.4 Voltage Control Loop

The combined current and voltage control loops are shown in Fig. 6.24, where the inner current control loop is enclosed by the outer voltage control loop. The functioning of the current control loop was presented in the previous subsection. The outer voltage control loop as shown in Fig. 6.24 functions to regulate the mean battery potential of the 20 lead-acid batteries used in the dc-dc converter circuit.

The transfer function $F_p(s)$ shown in Fig. 6.24 denotes the plant portion of the dc-dc converter in order to obtain a relationship between the dc bus current and the state of charge of the batteries. The battery voltage feedback circuit has a transfer function $J(s)$ and the transfer function $F_c(s)$ denotes the compensation circuit used for the outer voltage control loop.

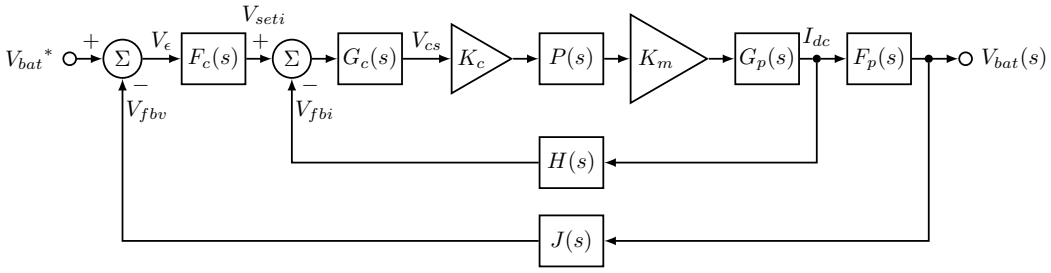

Figure 6.24: Voltage and current control loop block diagram.

Either the converter's batteries, the load connected between the dc bus rails, or both, are responsible for sinking the current flowing into the dc bus from the inverter. Since the load is not permanently connected, current will flow into the batteries, thus charging them. The batteries have a maximum floating use potential of 13.6 V to 13.8 V per battery which should not be exceeded. For the safety of the batteries the voltage control loop will strive to keep the batteries charged to a maximum mean potential of 13.6 V per battery, thus 272 V in total.

With reference to Fig. 6.12 and Fig. 6.24 the plant portion of the converter circuit is derived next. The 40 Ah batteries will take hours to fully charge and thus simulating their true response with respect to the current they sink requires an extremely long simulation. For time domain analysis the battery was approximated as a constant voltage source in series with a resistor and hence the total battery voltage v_{bat} is given by

$$v_{bat} = V_B + i_L R_{in}, \tag{6.52}$$

where V_B is the nominal battery voltage, i_L is the mean battery and inductor current, as defined in Fig. 6.1, and R_{in} is the internal battery resistance. The nominal voltage V_B will be adjusted in the time domain simulation over a period of a few seconds to ensure the voltage control loop responds correctly to a change in battery voltage.

For frequency domain analysis the battery was modelled as a large capacitor in series with a resistor. From first principles it is known that electrical charge is equal to voltage multiplied by capacitance ($Q = CV$) and one ampere-hour equals 3600 coulombs of charge. The value of the capacitor C_b representing the battery is thus approximated by

$$C_B = \frac{Q}{V_B} \approx \frac{3600 \times 40}{12 \times 20} = 600 \text{ F}. \tag{6.53}$$

The internal resistance of the twenty batteries R_{in} is approximated as 5 times the resistance of the batteries when fully charged, thus 0.95 Ω.

The mean dc bus current I_{dc} is related to the mean battery and inductor current I_L by

$$D_1 = \frac{I_{dc}}{I_L} = 0.6857, \tag{6.54}$$

as given in (3.3) and repeated here for convenience. The transfer function for the battery voltage with respect to the dc bus current is given by

$$F_p(s) = \frac{V_{bat}}{I_{dc}} = \frac{1}{D_1}\left(\frac{1}{sC_B} + R_{in}\right) = \frac{1 + sC_BR_{in}}{sD_1C_B}. \tag{6.55}$$

The battery voltage is measured by means of a fully differential amplifier as shown in Fig. 6.25 to provide the feedback voltage v_{fbv}. Two capacitors were added to the differential amplifier to form a low-pass filter that is used to reduce the noise on the measured signal.

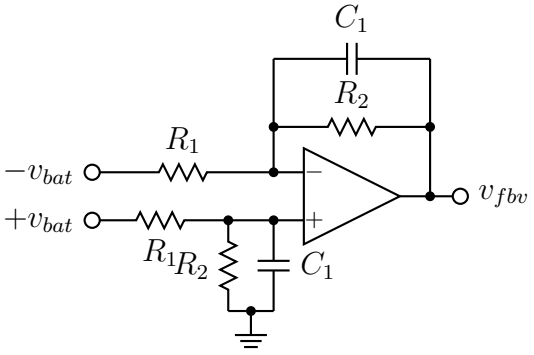

Figure 6.25: Battery voltage feedback circuit.

At a battery reference voltage $V_{bat}{}^*$ of 5 V the measured battery voltage should rise gradually to 272 V. The amplifier thus acts as an attenuator with a gain factor of $\frac{5}{272}$. The values chosen for R_1 and R_2 are 446 kΩ and 8.2 kΩ respectively. The capacitor C_1 is chosen as a 100 nF ceramic capacitor. The low pass filter's corner frequency is calculated using (6.47) as 194 Hz.

The transfer function for a low pass filter was already derived in (6.46). With reference to Fig. 6.24, the transfer function of the voltage feedback circuit is denoted $J(s)$ and thus $J(s)$ is given by

$$J(s) = \frac{R_2}{R_1}\left(\frac{1}{1 + sC_1R_2}\right). \tag{6.56}$$

The voltage control loop compensation amplifier is denoted $F_c(s)$. The block diagram shown in Fig. 6.24 can be reduced to the block diagram shown in Fig. 6.26 where the inner current control loop is replaced by the closed-loop transfer function $G_{cl}(s)$ derived in (6.50).

With reference to Fig. 6.26, the open-loop transfer function of the voltage control loop $F_{ol}(s)$ is

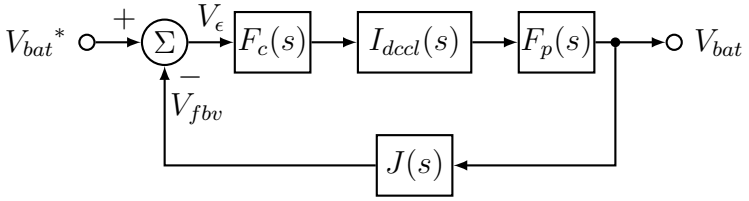

Figure 6.26: Reduced voltage and current control loop block diagram.

$$F_{ol}(s) = \frac{V_\epsilon(s)}{V_{fbv}(s)} = F_c(s)G_{cl}(s)F_p(s)J(s), \tag{6.57}$$

and the closed-loop transfer function $F_{cl}(s)$ is

$$F_{cl}(s) = \frac{F_c(s)G_{cl}(s)F_p(s)}{1 + F_c(s)G_{cl}(s)F_p(s)J(s)}. \tag{6.58}$$

The bode plot of the open-loop response $F_{cl}(s)$ without the transfer function of the compensation amplifier present is shown in Fig. 6.27. The frequency response shows a unity crossover frequency of approximately 10^{-5} Hz which is very low. The desired speed response of the voltage control loop is in fact very slow since the battery voltage will change over a period of minutes to hours. A slight gain can however be added to speed up the voltage control loop frequency response to approximately 0.01 Hz.

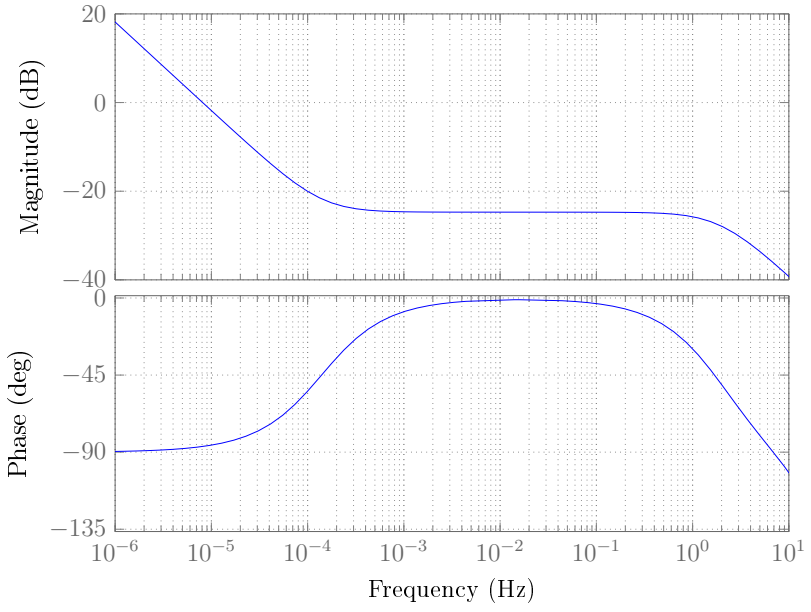

Figure 6.27: Bode plot of the open-loop frequency response of the voltage control loop without compensation.

The ability of the batteries to store charge allows it to act as a large capacitor which already provides an integrator as shown in Fig. 6.27, thus the voltage control loop has theoretical infinite gain at dc. A low-pass filter with gain and a very low corner frequency is selected as the compensator to ensure the current set-point V_{seti} is never changed abruptly. The circuit looks identical to Fig. 6.25 with R_1, R_2 and C_1 equal to 22 kΩ , 470 kΩ and 100 μF, respectively. The open- and closed-loop response of the voltage control loop are shown in Fig. 6.28.

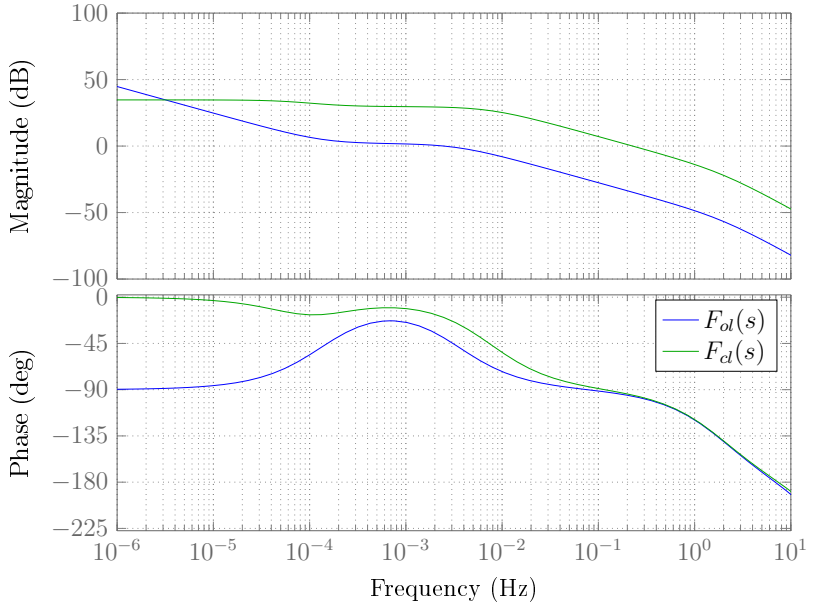

Figure 6.28: Bode plot of the open- and closed-loop frequency response of the voltage control loop.

From Fig. 6.28 the gain and phase margins are given by 75.7 dB and 140° respectively. The unity crossover frequency increased to 0.0025 Hz. The closed-loop response has a dc gain of 34.71 dB corresponding to a loop sensitivity of 54.33 V of battery voltage per volt of excitation applied to the voltage set-point V_{setv}. At a maximum set-point voltage of 5 V the corresponding battery voltage will rise to 272 V, as designed for. It should be noted, however, that regardless of the battery voltage measured by the circuit of Fig. 6.25, the battery charging current will never exceed a mean value of 10 A due to the action of the dc-dc converter.

The frequency domain analysis thus indicates that both the current and voltage control loops are stable. The complete circuit schematic for the inverter control board is given in Appendix A.2.2.

6.3 Summary

The detailed operation of the bidirectional inverter circuit and asynchronous generator were presented in this chapter. The switching and conduction losses for the chosen IGBT module were calculated numerically. The design and implementation of the inverter circuit's safety features were presented, amongst which are over-temperature, overcurrent and overvoltage protection. A detailed design of the inverter control circuit was also presented where two control loops, an inner and outer control loop, were used to regulate the dc bus current and battery voltage, respectively. Frequency domain analysis showed both control loops to be stable. The time domain equations describing the inverter operation were derived and the simulations are presented in the next chapter, along with the measured results from the manufactured prototype circuit.

Chapter 7

Inverter Simulation and System Integration Test Results

This chapter contains the simulated and measured test results of the integrated dc-dc converter and inverter circuit. The inverter circuit, designed in the previous chapter, is modelled and simulated in the time domain along with the generator detailed in Chapter 5. The simulated circuit is compared to the manufactured prototype circuit and the results are discussed. The implemented inverter safety features were tested and observations are presented.

The test set-up for the integration of the inverter and converter circuits is also described in this chapter. The measured battery voltage is compared to the measured dc bus current to validate the system integration and to demonstrate the practical operation of the completed circuit.

All time domain simulations were implemented in MATLAB where the relevant differential equations were once again solved using the iterative Euler method.

7.1 System Integration

The operation of the dc-dc converter prototype circuit (with and without a load connected to the dc bus) was already presented and discussed in Chapter 4. The inverter circuit was designed to operate from the regulated positive and negative dc bus rails provided by the dc-dc converter. The inverter control circuitry modulates the voltages applied to the asynchronous generator stator terminals and in return the generator supplies current to the dc bus through the inverter circuit at a constant negative slip of -5.47 %. The dc-dc converter's batteries are responsible for sinking the dc bus current flowing into the converter's dc bus terminals.

7.1.1 Test Set-Up

The test set-up for the complete system is shown in Fig. 7.1. The prototype inverter circuit is located on the left-hand side of the table shown in Fig. 7.1, while the prototype dc-dc converter circuit is placed on the right-hand side of the table. The 60 Ω , 2.1 kW load is placed between the two prototype circuits.

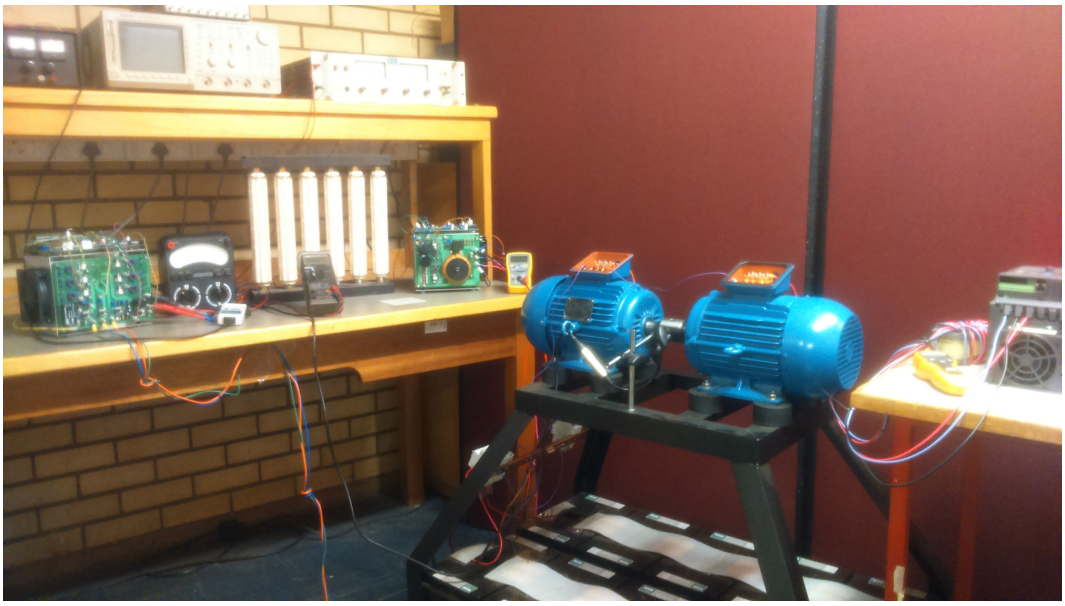

Figure 7.1: Test set-up for generator and battery interface circuit.

The inverter circuit is constructed in a similar manner to the dc-dc converter circuit. The control board is mounted on top of the power board connected to the heat sink. A small 12 V fan is also mounted to the side of the heat sink and control board. The detailed inverter PCBs are given in Appendix B.2. Both the inverter control and power boards are powered from a 12 V bench power supply through a DKE10A-15 converter.

The two induction machines (one to drive the other) are mounted on top of the trolley as shown in Fig. 7.1. The VSD controlling the induction motor operation is located to the right of the two machines.

The measurements for the system operation were obtained using an Agilent Technologies oscilloscope, LEM current probe, multimeter and Avometer, depending on the type of measurement required.

7.1.2 Start-Up Procedure

The inverter control circuit is switched on first (before the dc-dc converter circuit). The dsPIC ensures the inverter circuit will remain idle (not switching)

until it receives at least two magnetic pick-up interrupts to prevent the inverter from loading the dc-bus before it is fully charged.

Next, the dc-dc converter is switched on and the dc bus is charged to 355 V as presented in Chapter 4. The VSD system driving the induction machine used to simulated airflow through a turbine is switched on last. The generator shaft starts to turn, generating magnetic pick-up interrupts at one of the input channels of the dsPIC. The inverter control circuitry responds by generating PWM signals to turn on the IGBTs of the inverter, thus powering the generator.

7.2 PWM Generation and Gate Signals

The generation of the six PWM signals to drive each of the IGBTs were described and simulated in the previous chapter. The measured PWM generation results are presented in this section as well as the measured IGBT gate signals.

7.2.1 Reference Waveforms

The modulator reference waveforms are generated by the dsPIC DSP and the sinusoidal output waveforms are provided by a DAC, connected to the dsPIC as detailed in Section 6.2.2. As soon as the inverter control circuit is switched on, the battery voltage is measured and the dc bus current set-point is adjusted as a function of the battery voltage.

The nominal battery voltage is 12 V and when fully charged it can reach a nominal value of 12.6 V, hence the initial measured battery voltage will always remain below 260 V (13 V per battery). The control circuit will produce a maximum current set-point (5 V), thus demanding 5.7 A of dc bus current, if the measured voltage is below 260 V due to the gain provided by the voltage control loop's compensation amplifier.

Once the magnetic pick-up senses the generator shaft frequency has exceeded 7 Hz, the orange warning LED switches off and the amplitudes of the sinusoidal modulator reference waveforms slowly increase as shown in Fig. 7.2. The maximum amplitude of a waveform is dependent on the speed of the generator shaft and the magnitude of the control signal v_{cs}, generated by the current control loop's compensation amplifier.

At a shaft frequency of 25 Hz and a maximum v_{cs} control signal magnitude of 5 V, the maximum allowed amplitude V_c of the sinusoids are calculated using (6.39) as 1.92 V (3.84 V peak-to-peak), due to the scaling factor K_c defined in Section 6.2.2. Recall, by scaling the amplitudes of the modulator reference waveforms with respect to the generator shaft speed, the amplitudes of the fundamental stator voltages are also scaled and thus the generator is operated below or at rated flux. Saturation currents within the generator are thus avoided. The measured modulator sinusoids are shown in Fig. 7.3.

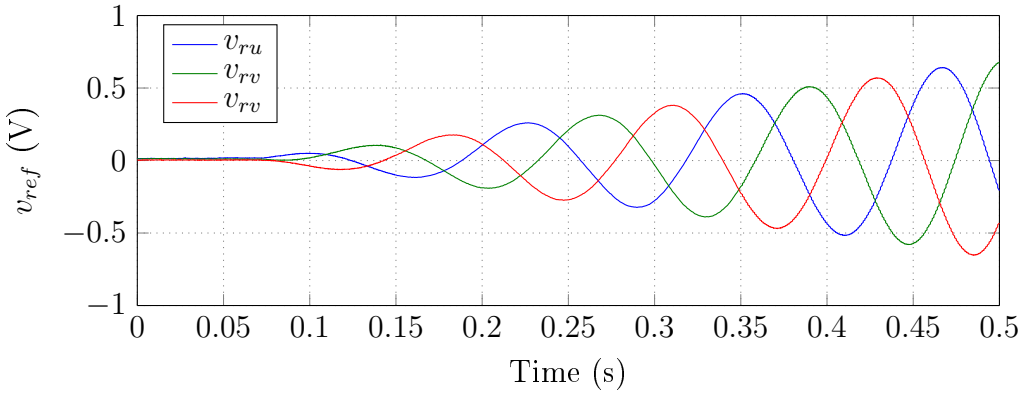

Figure 7.2: Measured modulator reference waveforms at an increasing generator shaft speed.

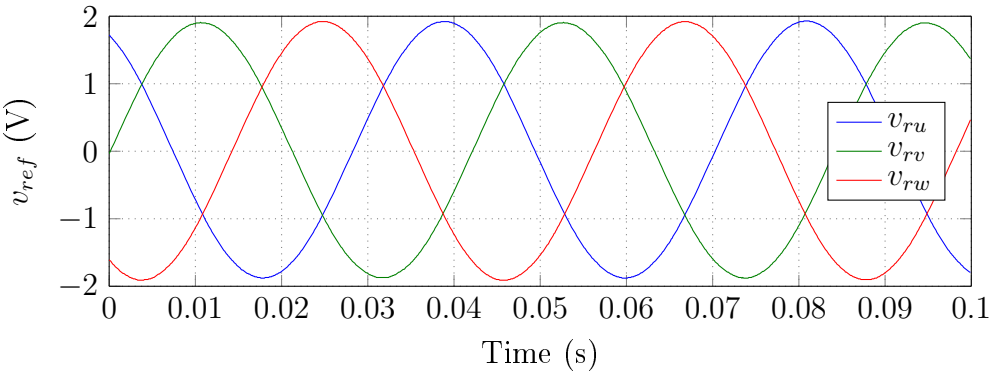

Figure 7.3: Measured modulator reference waveforms at a shaft frequency of 25 Hz.

The measured peak-to-peak voltages of the three waveforms shown in Fig. 7.3 are 3.83 V, 3.78 V and 3.80 V, respectively, closely matching the designed voltage of 3.84 V. The amplitudes of the three sinusoids are close to, but not identical to each other. This indicates a small margin of error introduced by the op-amp and resistor circuit that is used to remove the dc offset and add a gain of 2 to each of the DAC outputs. The gain of each sinusoid is thus slightly greater or lower than two, resulting in the small voltage error. The resulting phase currents will thus also vary ever so slightly in error. The small error in current and voltage will not stop the generator from operating as required.

The measured frequency of each of the waveforms shown in Fig. 7.3 is 23.7 Hz corresponding to a slip of -5.47 %, thus matching the designed slip of -5.47 %.

Similarly at a shaft frequency of 50 Hz, the maximum allowed sinusoidal voltage is 7.69 V peak-to-peak. The measured sinusoidal modulator reference

waveforms at a shaft frequency of 50 Hz are shown in Fig. 7.4. The peak-to-peak voltages are measured as 7.65 V, 7.58 V and 7.6 V, respectively. The voltages are close to the designed maximum voltage of 7.69 V. The reference waveform frequencies are measured as 47.4 Hz corresponding to the designed slip of -5.47 %.

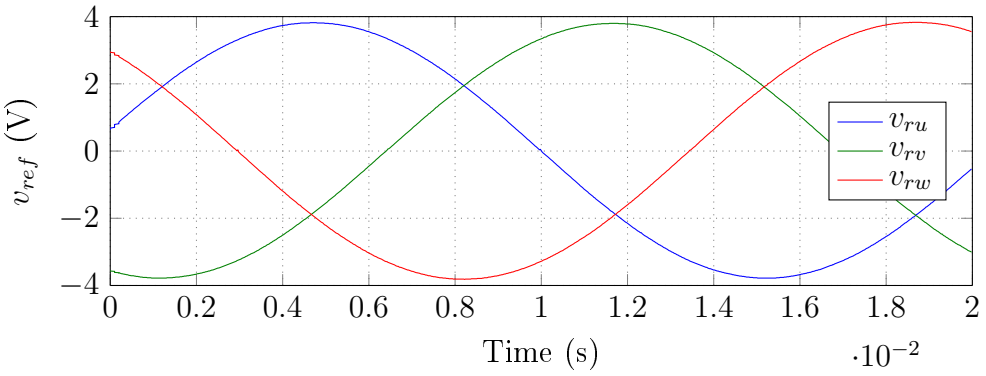

Figure 7.4: Measured modulator reference waveforms at a shaft frequency of 50 Hz.

The dsPIC and DAC are seen to function as designed and deliver the correct modulator reference voltage waveforms at various measured generator shaft speeds. From Fig. 7.3 and Fig. 7.4 it can be seen that the digitally generated sinusoids look very much like analog signals, indicating the resolution chosen for the digital sinusoids is adequate.

Lastly, when the generator shaft frequency exceeds the maximum frequency of 75 Hz, the orange warning LED switches on and the reference waveforms gradually reduce until reaching peak-to-peak values of zero.

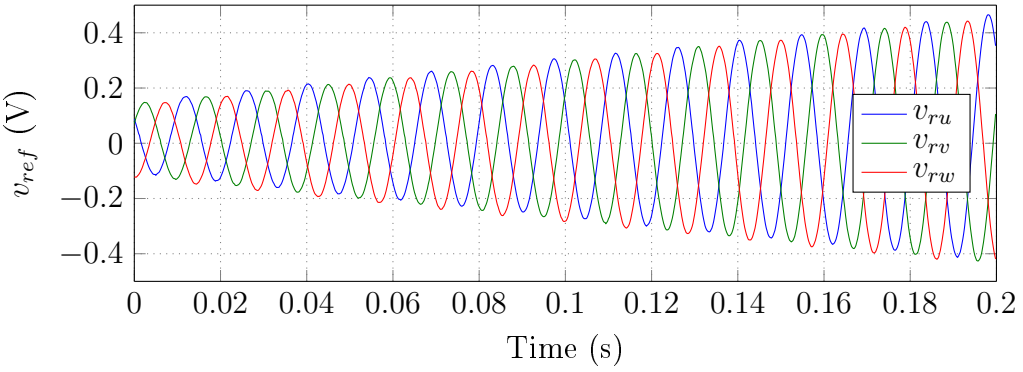

Figure 7.5: Measured modulator reference waveforms after the operating shaft speed range was exceeded.

Similarly when the shaft frequency was slightly reduced to a value below 75 Hz, the reference waveforms were seen to gradually return to an amplitude of 5 V as shown in Fig. 7.5. The warning LED switched off and normal switching operation continued.

7.2.2 Triangular Carrier Waveform

The triangular carrier waveform used for comparison with the sinusoidal reference waveforms, was designed to have a frequency of 20 kHz and a peak-to-peak voltage of 12 V. The measured carrier waveform is shown in Fig. 7.6.

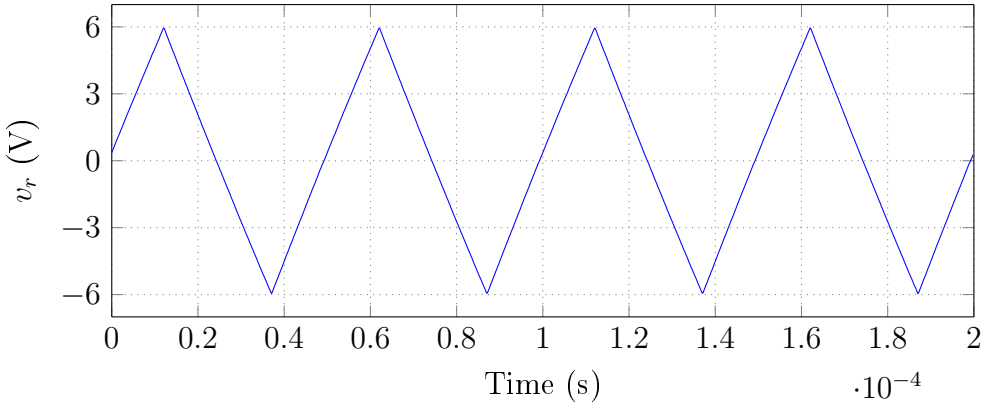

Figure 7.6: Measured triangular carrier waveform.

The measured frequency is 20 kHz and the peak-to-peak voltage is 11.9 V. The amplitude of the triangular wave is thus 5.95 V. The measured result compares extremely well to the designed carrier waveform detailed in Section 6.1.

7.2.3 Switching Signals

The measured PWM switching signals generated by the inverter control circuitry for the IGBTs in one half-bridge are shown in Fig. 7.7.

The switching signal of S_1 is complementary to S_2, as designed. At the instance of the measurement the duty cycle for S_1 was 68.4 % and 26.6 % for S_2. The implementation of the dead-time can clearly be seen in Fig. 7.7 due to the small time period during which both switches are off. The dead-time was set to 1.2 μs and was chosen as such to avoid any IGBT shoot-through currents.

Similar PWM signals were generated for the other two half-bridges containing switches S_3 through S_6. The duty cycles vary sinusoidally and in phase with the modulator reference voltage waveforms, as expected.

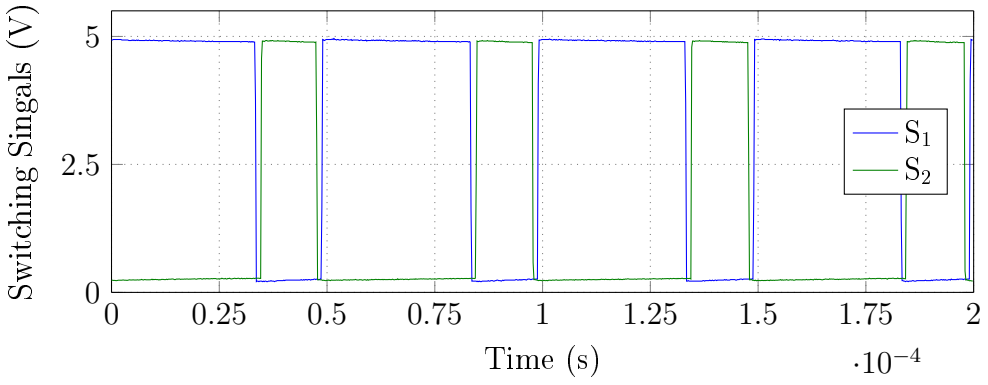

Figure 7.7: Measured PWM switching signals for one inverter half-bridge.

At a maximum reference waveform amplitude of 5 V and a 5.95 V ramp wave amplitude, the maximum modulation index is 0.84. From (6.8) the maximum duty cycle is thus limited to 92 %.

7.2.4 IGBT Gate Signal

The push-pull oscillator circuit used to power the gate driver IC that communicates the switching signal to the gate of the IGBT, was determined to oscillate at a frequency of 309 kHz. The optocoupler supply voltage was measured as 16.4 V, close to the designed voltage of 16.5 V.

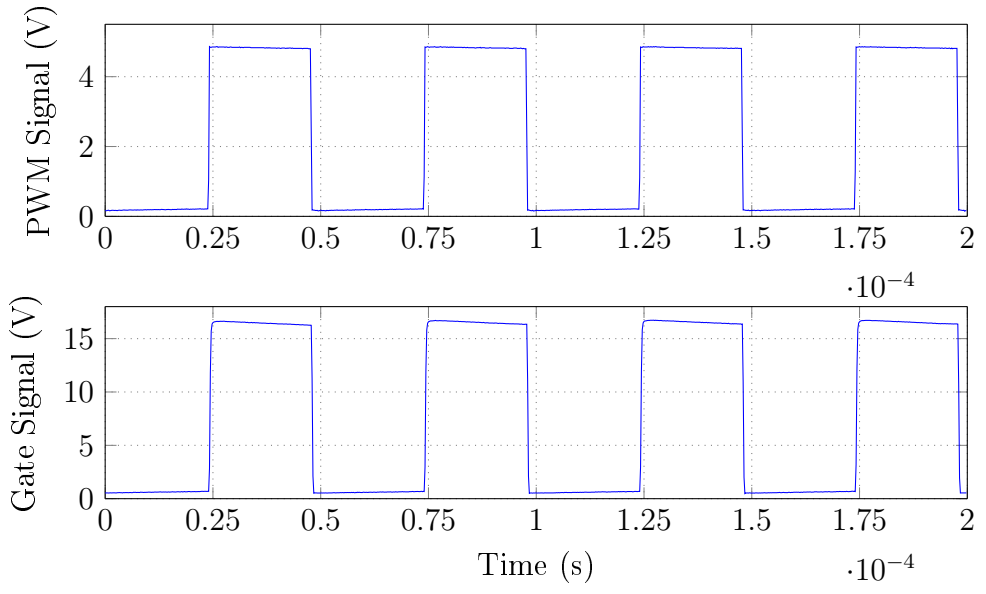

Figure 7.8: Measured controller and gate PWM switching signals.

At a generator shaft frequency below 7 Hz or above 75 Hz, the duty cycle of all the switches change to a constant value of approximately 50 %, since the reference waveforms have reduced to a constant zero volt signal. The measured PWM switching signal for S_1, as well as the signal at the gate of the corresponding IGBT, are shown in Fig. 7.8 at a generator shaft frequency below 7 Hz.

The measured duty cycles for both the PWM control signal and the gate signal were 47.6 %. Due to the dead-time the duty cycles are slightly lower than the ideal 50 %. The signal at the gate of the IGBT has a maximum voltage of 16.3 V corresponding to the gate driver IC supply voltage of 16.4 V.

7.3 Current Simulation and Test Results

The PWM gate drive signals produce PWM voltages at the three pole points of the inverter. These voltages are also applied to the generator stator terminals with their fundamental component at a lower frequency than the measured shaft frequency. Due to the constant -5.47 % slip operation, current is induced in the rotor of the generator and current will flow out of the generator into the dc bus.

The outer voltage control loop will demand a current of no greater than 5.7 A when a 2 kW load is connected between the dc bus rails, thus no power flows into the batteries to allow them to charge. As soon as the load is removed or its resistance increases, current flows into the batteries and the battery voltage rises to above 260 V. In return less current is demanded by the voltage control loop and the battery voltage progressively settle. The batteries are further charged slowly and the mean dc bus current gradually decreases, under the control of the two control loops.

The phase currents and dc bus current were simulated in MATLAB at the maximum allowed mean dc bus current as well as at a lower dc bus current, such as while the batteries are charging. The results are presented in this section and the time domain analysis showing the stability of the system is also discussed. The corresponding measurements of these currents are presented and compared with the simulated results.

Without a 2 kW load connected between the dc bus rails, the dc bus current is shown to flow into the converter to charge the batteries.

7.3.1 Inverter Phase Currents

Initially no load is connected between the dc bus rails. The battery voltage begins to rise as soon as the bus current rises, since the batteries are being charged. The inverter phase current measurements were taken once the battery voltage started to settle at a voltage of 266.1 V and a mean dc bus current

of 3.3 A. For comparison purposes the simulation was repeated under these conditions.

The simulated phase currents are shown in Fig. 7.9 at a set-point voltage corresponding to a mean dc bus current of 3.3 A and a generator shaft frequency of 50 Hz. The corresponding measured phase currents are shown in Fig. 7.10.

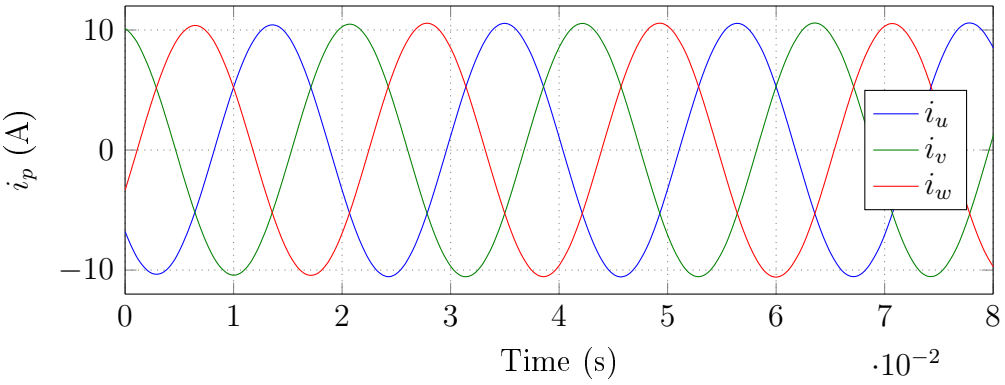

Figure 7.9: Simulated inverter phase currents at a 3.3 A dc bus current set-point.

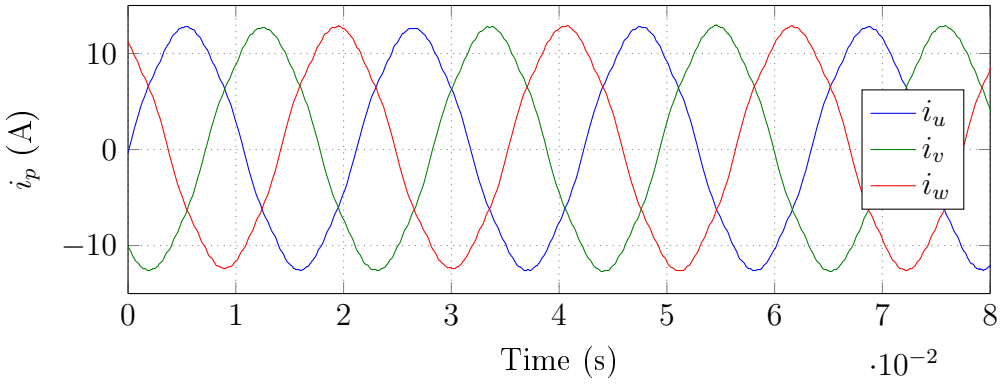

Figure 7.10: Measured inverter phase currents at a measured dc bus current of 3.3 A.

The simulated phase currents each have an rms value of 7.5 A and a frequency of 47.4 Hz. The rms values of the three measured phase currents are 8.99 A, 8.89 A and 8.95 A, respectively. As indicated by the measured modulator reference waveforms, the phase currents will also vary slightly in magnitude. The frequency of the measured phase currents are 47.5 Hz each. From Fig. 7.10 it can be seen that the measured phase currents are not pure sinusoids. This

is due to the fact that the inductance of the generator is, in reality, a function of the currents passed through the generator windings due to the non-linear magnetic permeability of the rotor and stator core material. As a general rule the permeability of the ferromagnetic core material is seen to decline as the generator line currents increase. We thus observe the distorted sinusoidal phase currents in response to the application of sinusoidal fundamental phase voltages to the generator stator terminals.

Both the simulated and measured phase currents indicate a constant generator slip of approximately -5.47 %, as designed for. The rms value of the simulated and measured phase currents does however differ by approximately 1.5 A, indicating the equivalent generator impedance is lower than the impedance approximated by the equivalent induction machine model derived in Chapter 5. A margin of error was expected since the parameters of induction machines change with a change in temperature and operating frequency (slip) [42], [43].

The simulated and measured phase current ripple are shown in Fig. 7.11 and Fig. 7.12, respectively. The simulated current ripple has a peak-to-peak value of 0.22 A. The measured current ripple has a peak-to-peak value of 0.356 A. The measured current ripple is larger than the simulated current ripple confirming the statement that the true machine inductance is lower than the values calculated in Chapter 5 from the approximate machine model.

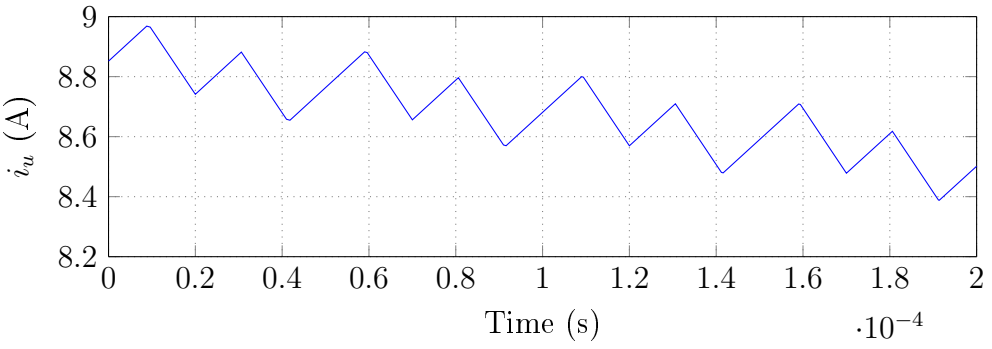

Figure 7.11: Simulated inverter phase current ripple.

The frequency of both the simulated and measured current ripple is 20 kHz corresponding to the 20 kHz switching frequency of the IGBTs. The measured ripple current is shown to have a significant amount of high-frequency noise superimposed on the signal. This noise is not real and is simply due to the noise picked up by the LEM current probe while taking the measurement. The two induction machines, VSD, dc-dc converter and inverter all operating at different frequencies and thus a significant amount of noise is produced, which is easily picked up by measuring equipment. One of the most significant sources of radiated noise was determined to be the commercial VSD used to control the motor coupled to the shaft of the generator.

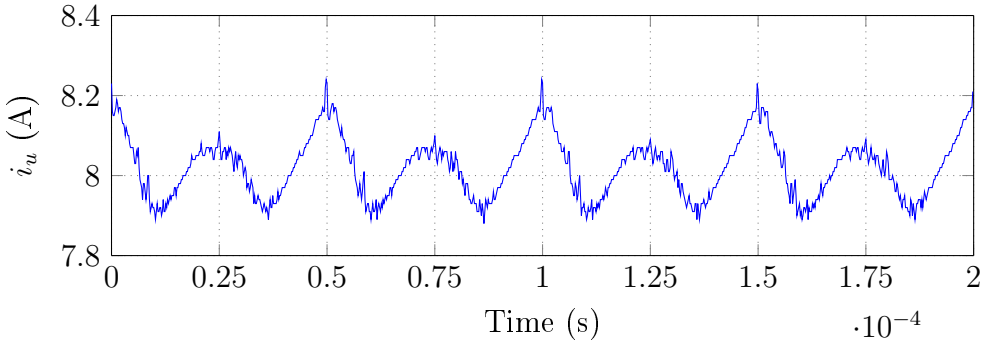

Figure 7.12: Measured inverter phase current ripple.

The simulated modulator reference waveform for switches S_1 and S_2 is shown in Fig. 7.13, along with the corresponding phase current i_u at a mean dc bus current of 3.3 A. The modulator reference voltages are in phase with the fundamental component of the inverter phase voltages, if the modulator circuit is considered ideal. The modulator reference waveforms can thus be used to determine the phase angle between the phase currents and voltages. As seen from Fig. 7.13 the current is leading the modulator reference voltage and the phase angle was determined from the simulation as 35.82°.

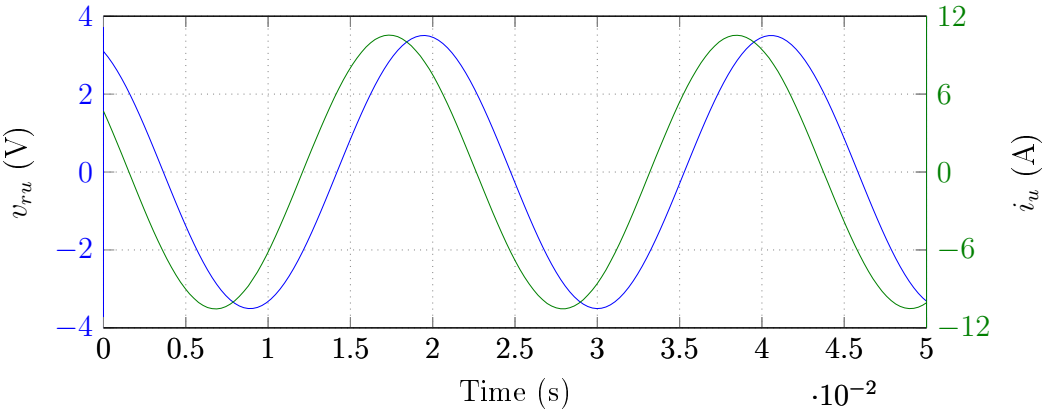

Figure 7.13: Simulated modulator reference voltage and phase current for one inverter half-bridge.

The measured phase current i_u and the modulator reference waveform for switches S_1 and S_2 are shown in Fig. 7.14. Since the inverter phase voltage waveforms are modulated, their fundamental waveforms are not easily measured. Although the modulator circuit itself is not ideal, the phase shift between the fundamental phase voltages and currents are approximately equal to the phase shift between the measured modulator reference waveforms and

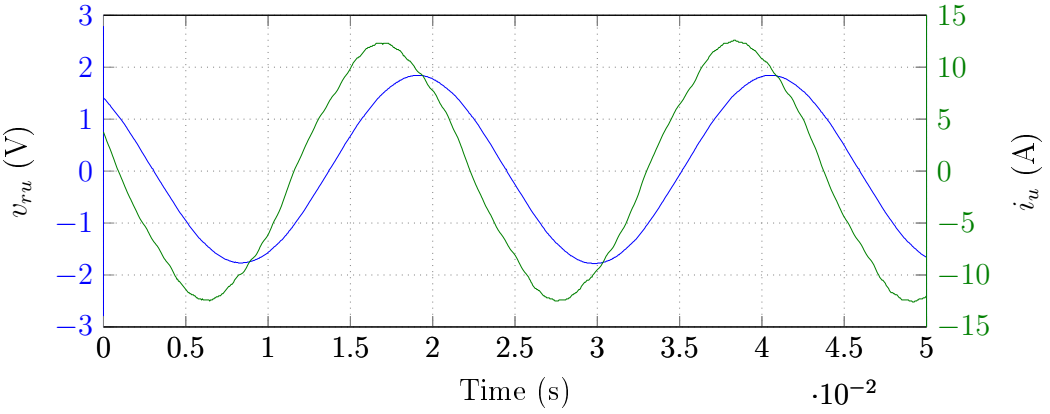

Figure 7.14: Measured modulator reference voltage and phase current for one inverter half-bridge.

the phase current waveforms. From Fig. 7.14 the current is shown to lead the modulator voltage by 35.88°.

The amplitude of the modulator reference waveform is seen to differ for the simulated and measured case shown in Fig. 7.13 and Fig. 7.14, respectively. This is because the dc bus current is regulated to 3.3 A and, as already shown, the measured phase currents are larger than the simulated phase currents. Thus, a lower modulator reference voltage is required to produce 3.3 A of current flowing in the dc bus for the measured case.

Once the 2.1 kW load is connected, the battery voltage reduces to below 260 V since the batteries as well as the generator is used to supply power to the load. The set-point generated by the voltage control loop increases to 5 V (5.7 A). At a shaft frequency of 34 Hz the corresponding measured modulator voltage and phase current are shown in Fig. 7.15.

From Fig. 7.15 the modulator reference voltage is shown to peak at 2.5 V and the measured frequency is 32.1 Hz. The maximum allowed reference voltage is 2.6 V at a shaft frequency of 34 Hz. The corresponding phase current has an rms value of 11.99 A. The power angle is measured as 36.9°. The phase shift is thus seen to remain constant with a change in frequency when compared to the power angle of 35.88° at a shaft frequency of 50 Hz.

The amplitudes of the phase currents will remain reasonable constant over a wide generator shaft speed range since both the fundamental stator voltages and generator impedance change with speed. From measurements it was seen that at low shaft speeds (below approximately 20 Hz) this voltage and impedance relationship does not remain constant and the amplitude of the phase currents will change significantly as a function of the shaft speed.

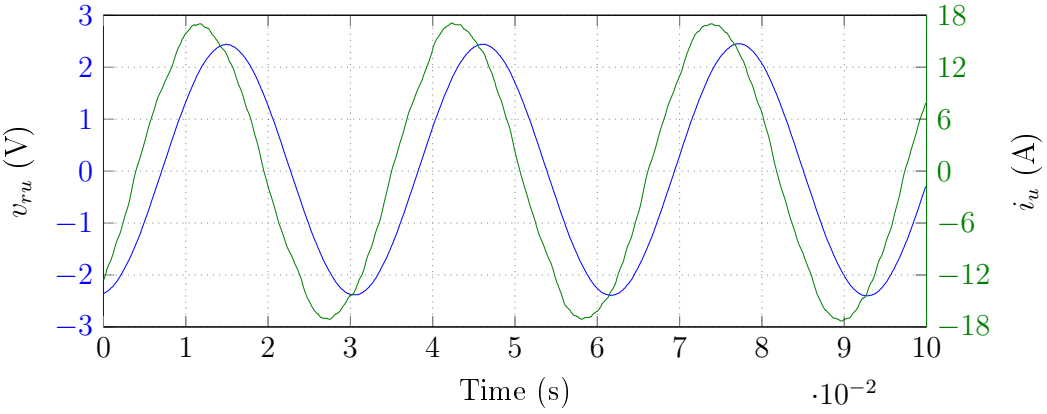

Figure 7.15: Measured modulator reference voltage and phase current at a shaft frequency of 34 Hz.

7.3.2 Bus Current

The time domain analysis of the dc bus current during start-up is shown in Fig. 7.16 for a maximum current loop set-point of 5 V. The simulation was conducted at a shaft frequency of 50 Hz. The amplitudes of the modulator reference waveforms were gradually increased as discussed in Section 7.2.1. The dc bus current is shown to increase with an increase in the applied inverter phase voltages, as expected. After 2.42 s, the dc bus current is shown to reach the desired mean dc bus current value of 5.7 A. A small current overshoot of 0.4 A follows with the dc bus current thus peaking at 6.1 A. After a total of 2.6 s the dc bus current is shown to have settled to the desired value of 5.7 A.

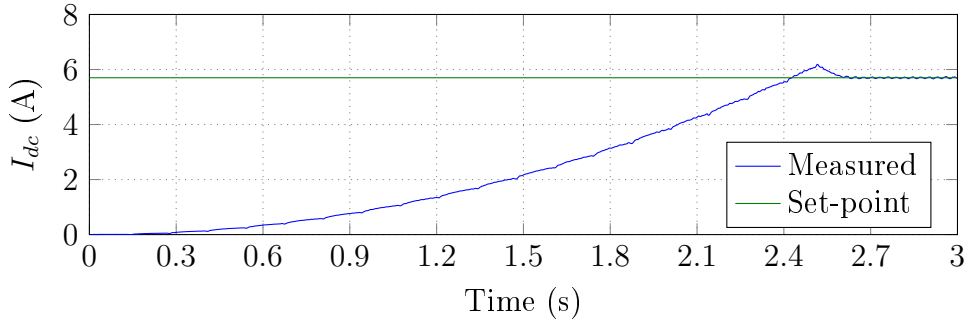

Figure 7.16: Simulated dc bus current during generator start-up.

The time domain analysis shows the dc bus current will settle at the desired current set-point without a large current overshoot (less than 7.1 %). The system is seen to be stable and able to supply the current required by the outer control loop.

The VSD controlling the motor (used to turn the generator shaft) was set to accelerate the frequency of the stator voltages applied to the motor over a period of 10 s to avoid saturation currents in the motor. The slow acceleration of the generator shaft combined with the gradual increase of the amplitudes of the modulator reference waveforms cause the measured dc bus current to ramp up slowly and with a maximum current overshoot of approximately 0.1 A to peak at 5.8 A. The motor is decelerated in a similar manner using the VSD.

In practice the dc bus current set-point will never experience a step response after start-up, since the outer voltage control loop is set to react very slowly (due to the batteries charging slowly) and hence the set-point generated by voltage control loop will change gradually, allowing the dc bus current to follow. This response is detailed in the next section.

The measured dc bus current under steady state conditions is shown in Fig. 7.17 at a maximum set-point of 5 V, corresponding to 5.7 A, and a generator shaft frequency of 50 Hz. The mean value is measured as 5.66 A which closely match the desired value of 5.7 A. The error is due to a small inaccuracy in the current sensing circuit. With a regulated 355 V dc bus, the power requirement of 2 kW is still met. The inverter and generator circuit is thus able to supply 2 kW of power to the dc bus.

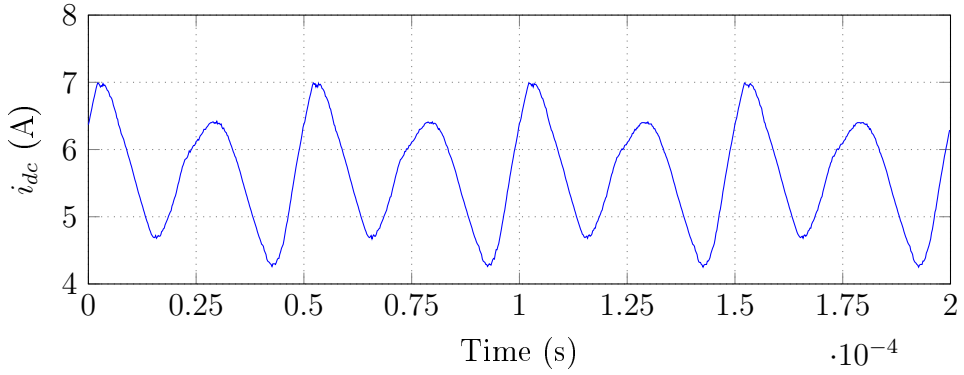

Figure 7.17: Measured dc bus current at the maximum set-point current.

The dc bus current is shown to have a fundamental frequency of 20 kHz with a 40 kHz component also present. The inverter is switching at 20 kHz while the dc-dc converter is switching at 40 kHz accounting for the additional frequency component. The ripple in the dc bus current is seen to have a peak-to-peak value of 2.75 A. An increase or decrease in the amplitudes of the three inverter phase currents will result in a corresponding increase or decrease in the peak-to-peak dc bus current ripple.

Due to the difficulty in measuring the fundamental component of the inverter phase voltages, the inverter efficiency was not determined. A power analyser of some sort is required to accurately measure the efficiency of such

a circuit. The lab facilities available for this project did unfortunately not contain any power analysers.

The dc bus current was also measured whilst charging the batteries. The measurement was taken along with the already presented phase current measurements at a mean dc bus current of 3.3 A as shown in Fig 7.18. The ripple current has a peak-to-peak magnitude of 1.94 A, which is lower than that of the previous dc bus current measurement, as expected.

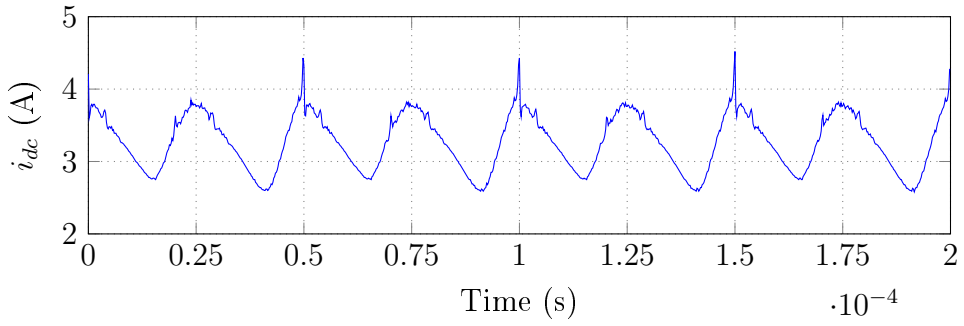

Figure 7.18: Measured dc bus current whilst charging the batteries.

The dc bus current control loop is shown to be stable and able to regulate the current flowing into the dc bus effectively. The power transfer requirement of 2 kW is also shown to be met by the prototype circuit.

7.3.3 Battery Current

The measured current flowing into the batteries at a mean dc bus current of approximately 3.3 A is shown in Fig. 7.19. The battery current is shown to have a mean value of 4.8 A and a peak-to-peak current ripple of 2.04 A at a frequency of 40 kHz.

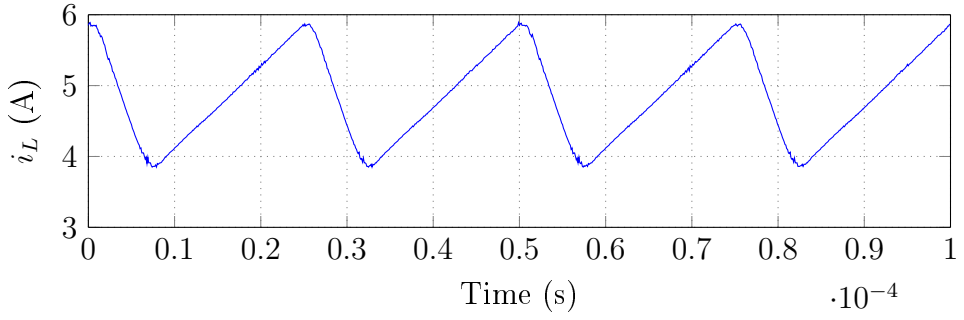

Figure 7.19: Measured battery current whilst charging the batteries.

The inductor current ripple is seen to be lower than the designed value of 2.25 A even if the inductor is experiencing greater magnetisation which would increase the current ripple. This is simply due to the battery voltage that increased to 266.1 V from the nominal value of 240 V (12 V per battery). The voltage across the inductor is thus less than before when switches Q_1 and Q_4 are closed, resulting in a smaller current ripple. The duty cycle of switches Q_1 and Q_4 are also seen to have changed slightly to 70 % as opposed to the previous value of 68.57 %.

The dc-dc converter is thus shown to be bidirectional since it can accommodate current flow to as well as from the dc bus. The results showing power flow from the batteries to the dc bus were already presented in Chapter 4.

7.4 Bus Current and Battery Voltage Relationship

The results of the outer voltage control loop used to regulate the battery voltage are presented in this section. As the battery voltage increases, the dc bus current should decrease until such point where the current supplied by the generator is just enough to keep the batteries at their floating use voltage of 272 V to 276 V. Both the simulated and measured response of the dc bus current with respect to the state of charge of the batteries are presented and described.

7.4.1 Simulated Response

The time domain simulation only deals with the electrical properties of the batteries, thus the batteries were modelled as a constant voltage source with an internal resistance, as detailed in Chapter 6. In order to observe the change in dc bus current as a function of the battery voltage in the simulation, the battery voltage (modelled as the constant voltage source) was increased linearly over a time period of 7 s.

To provide a better approximation of the battery's response to sinking current, the battery voltage was simulated to increase from 240 V (nominally 12 V per battery) to 265 V over a period of 3 s and then increase slowly to 272 V over the next 4 s. The results are shown in Fig. 7.20.

Initially the set-point current corresponds to 5.7 A as indicated in Fig. 7.20. The dc bus current is ramped up as explained in Section 7.3.2. At the same time the battery voltage is seen to rise gradually. After 3 s the battery voltage exceeds 260 V and the current set-point is shown to decline. The simulated dc bus current is seen to respond to the change in the current set-point. When the battery voltage reaches 265 V the batteries start charging at a lower rate. The current set-point is seen to also decline at this lower rate, with the dc bus current following its response. Once the battery voltage reaches the desired

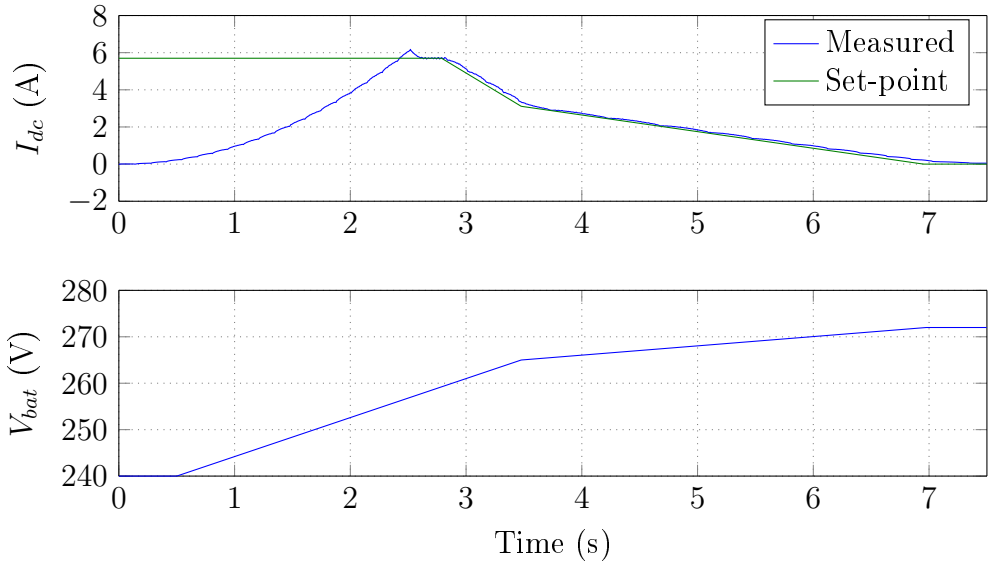

Figure 7.20: Simulated mean dc bus current and battery voltage.

value of 272 V, the current set-point reaches zero, thus demanding zero current. The dc bus current is also seen to reduce to the desired value of zero.

The time domain simulation predicts that both the voltage and current control loops of the inverter are stable.

7.4.2 Measured Response

Due to the time duration required for the batteries to charge, the measurement could not be obtained as a single measurement using an oscilloscope. The mean battery voltage was measured at regular intervals with a multimeter and the mean dc bus current was measured with an Avometer as well as as with a LEM current probe, to confirm the measurement. As soon as the generator started to deliver power to the dc bus (a load was not connected between the dc bus rails), the battery voltage was seen to increase rapidly to above 260 V. The results were taken from a battery voltage of 260 V and are shown in Fig. 7.21. The measurements were taken with the batteries drained beforehand to a value of approximately 11.92 V per battery.

The results given in Fig. 7.21 show the mean dc bus current does in fact decrease as the mean voltage of the batteries increases, as desired. Initially the dc bus current is seen to peak at 5.8 A while the dc bus voltage increases rapidly. The gain used in the voltage compensation amplifier is sufficient to demand 5.7 A of current up to a measured battery voltage of 260 V. Thereafter the demanded current is decreased as shown in Fig. 7.21.

The current is seen to drop at approximately the designed rate until the battery voltage reaches 265 V. Thereafter the battery voltage starts to settle

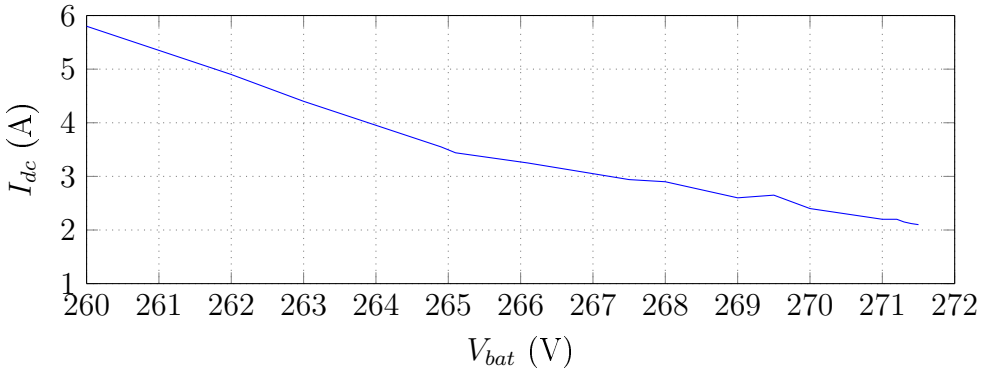

Figure 7.21: Measured mean dc bus current vs battery voltage.

and requires more current than predicted to continue charging the batteries. From Fig. 7.21 the voltage is seen to never reach exactly 272 V, it remains somewhere between 271 V and 272 V. Similarly the dc bus current is seen to reach a minimum value of approximately 2.1 A. The battery voltage and dc bus current thus reach equilibrium at these values. The equilibrium values can change with a change in temperature, since the storage capacity of batteries are temperature dependent.

The simulation predicted that the dc bus current will drop to zero at a battery voltage of 272 V. In practice the battery voltage will never actually reach 272 V but will remain very close to 272 V as long as the necessary current is supplied to keep it there, thus trickle charging the batteries. The internal resistance of the batteries as well as the efficiency of the converter causes the dc bus current to remain above zero in order to keep the batteries at their optimal floating use voltage of 272 V.

The last few measurements were taken approximately 30 minutes from each other. In total the batteries where charged for approximately 8 hours to reach a voltage of 271.5 V. If the batteries are charged even longer, the internal battery resistance will decrease even further and the required dc bus current will decrease slightly.

Overall the inverter control circuit is shown to be stable and provides the desired controller responses. The dc-dc converter prototype circuit was successfully integrated with the inverter prototype circuit. The mean dc bus current provided by the generator is successfully controlled as a function of the measured battery voltage, with the batteries connected to the dc-dc converter. The overall system is also shown to be stable under various operating conditions (with or without a load connected).

7.5 Safety Features Testing

The safety features detailed in Chapter 6 were implemented in the inverter prototype circuit. The soft turn-on and turn-off feature of the amplitudes of the modulator reference waveforms when the generator shaft speed exceeds the operating speed range (above 75 Hz or below 7 Hz), were already presented and discussed in Section 7.2.1. The correct LED also turned on to visually indicate why the generator cannot supply current to the dc bus.

A green LED was also mounted on the PCB containing the dsPIC. The LED was programmed to turn on and off at 0.5 s intervals. If the LED stops flashing it indicates the dsPIC is either not receiving power or has fallen into a continuous loop where the low priority interrupt to turn the LED on and off can never be reached. This provides a visual method to indicate if the control circuit is switched on and to see if the dsPIC itself is experiencing any major problems. The other safety features were also tested and is discussed in this section.

7.5.1 Over-Temperature Protection

The over-temperature detection was tested using an external input to simulate the temperature output from the thermistor circuit. At a voltage of 3.35 V (the designed threshold voltage) the over-temperature sensor tripped and the red LED was switched on by the dsPIC. At the same time all switching action was terminated as desired. The mean dc bus current was seen to drop and after a few seconds it reached zero. The switching action only resumed after the dsPIC was reset. Similarly the red LED only turned off once the dsPIC circuit was restarted.

7.5.2 Overcurrent Protection

The overcurrent protection is supplied by the gate driver IC (ACPL-332J) which detects the V_{ce} voltage of the IGBTs. The larger the currents through the collector of the IGBT, the higher the measured V_{ce} voltage. The IGBT module was tested before using it in the fully functional inverter circuit to see that the fault output from the gate driver IC tripped when large currents were flowing through the IGBT collector. The fault output was observed to change state thus indicating it functioned correctly.

Initially the dead-time for the IGBT switches was set to 800 ns. The inverter circuit was able to function as desired but after a while, when the IGBT module started to heat up, shoot-through currents were detected due to the increased turn-on and turn-off times of the switches. The overcurrent protection provided by the gate driver IC sent a fault signal to the dsPIC while activating the soft switch turn-off feature built into the chip. The orange LED was turned on by the dsPIC. Similarly as with the over-temperature

fault condition, the switching action was terminated. The control circuit was restarted to allow the switching action of the IGBTs to resume and to allow the LED to turn off. The dead-time was subsequently increased to 1.2 μs.

7.5.3 Overvoltage Protection

The overvoltage protection was tested using an external input to simulate the dc bus voltage feedback. As soon as the simulated scaled dc bus voltage exceeded 5 V, the output of the comparator was shown to change state, thus the overvoltage protection circuitry was triggered. The IGBT switching action was once again terminated as with the other protection features. The reverse biased diodes connected across the collector and emitter of each IGBT still provide a path for the generator current to flow, but as soon as the switching action of the IGBTs are terminated the voltage applied to the generator stator terminals are also terminated. With no voltage applied to the generator stator terminals the induced current immediately reduces and after a few seconds (less than 5 s) the mean dc bus current reaches zero.

The dc bus voltage will thus not rise to a high enough voltage to damage any of the components used in the inverter and converter prototype circuits. All of the high voltage components are rated to operate continuously at a voltage of at least 400 V. The IGBT switching action is resumed after the dsPIC is restarted.

7.6 Summary

The performance of both the inverter and dc-dc converter prototype circuits were presented in this chapter with the main focus on the integration between the two circuits. The test set-up and start-up procedure to test the complete system was described in detail. The generation of the gate-drive signals used to control the switching action of the IGBTs was presented using measurements. The inverter phase currents and dc bus current were presented in order to demonstrate the correct operation of the designed inverter current loop when compared to the simulated response. The measured battery current used to charge the batteries was given indicating that the dc-dc converter is in fact bidirectional. The test results showing the relationship between the mean dc bus current and measured battery voltage were presented and the integration of the dc-dc converter and inverter circuits were proven to be successful. The inverter protection circuitry was shown to function properly and provide the necessary protection for which it was designed.

Chapter 8

Conclusions

A summary of the work presented in this thesis along with the results are given in this chapter. Recommendations with regard to the research conducted are discussed and possible future work is considered.

8.1 Thesis Conculsions

A circuit that demonstrates the interface between an asynchronous generator, a battery of electrochemical cells, and an electrical load was proposed. This thesis presented the successful design and implementation of such a circuit.

The circuit was designed such that the battery connects to a dc bus through a bidirectional dc-dc converter, and the asynchronous generator connects to the same dc bus through a bidirectional inverter. A positive and a negative dc bus rail were used and the load was connected between the two bus rails.

The bidirectional dc-dc converter circuit was successfully designed to regulate the dc bus to 355 V rail-to-rail (within the design specification) by employing two control loops, an inner current control loop and an outer voltage control loop. The inner current control loop was used to control the amount of current flowing into or out of the converter's batteries as a function of the set-point generated by the outer control loop that regulates the dc bus voltage. Both frequency and time domain analysis confirmed the closed-loop stability of the system.

The converter was practically implemented by manufacturing PCBs to construct the prototype circuit. The converter circuit used a half-bridge topology consisting of MOSFETs as switches, which were controlled using pulse-width modulation. A two-stage soft-start circuit was successfully implemented to avoid in-rush currents during start-up through the reversed biased diodes of the MOSFETs.

The transfer of up to 2.1 kW of electrical power between the batteries and dc bus was demonstrated by powering a 2.1 kW load connected between the dc bus rails. The step response of the converter circuit was tested and excellent

transient response was demonstrated. Overall the simulated and test results compared extremely well. The converter also showed a high efficiency of 94 %.

The asynchronous generator, controlled by the inverter circuit, was successfully modelled in a computer simulation when compared to the given datasheet information.

The detailed design of the bidirectional inverter circuit used to interface the asynchronous generator and the dc bus was presented and implemented. The switching action of the IGBTs used in the inverter circuit were controlled using two control loops. The inner control loop was used to successfully control the magnitude of the current flowing into the dc bus while the outer control loop was used to regulate the converter's battery voltage. Both frequency and time domain analysis showed the closed-loop inverter system to be stable.

A dsPIC digital signal processor was used along with a digital-to-analog converter to produce the required sinusoidal modulator reference waveforms for the inverter switches. A magnetic pick-up was used to determine the speed of the generator shaft and the result was processed inside the dsPIC. The generator was shown to function as desired when operated at a constant slip of -5.47 % using current as well as Volt/Hertz control. The generator was able to supply 2 kW of electrical power to the dc bus when a load was connected between the bus rails.

The integration of the dc-dc converter circuit and inverter circuit was successfully implemented. The generator was shown to supply power to the dc-dc converter circuit in order to charge the batteries to their optimal floating use voltage of 272 V. The bidirectional capability of the dc-dc converter circuit was thus proven.

The test results showed that as the battery voltage increased, the demanded dc bus current decreased, indicating the inverter control loops functioned as desired. The dc bus current reached a minimum demanded value of 2.1 A, which was the necessary current required to keep the battery voltage at approximately 272 V, thus trickle charging the batteries.

The prototype circuits showed that the induction generator can be controlled as a function of the dc-dc converter's battery voltage by making use of the presented dc-dc converter and inverter circuits. The overall system performance was shown to meet all the design specifications.

8.2 Recommendations and Future Work

The prototype circuit was tested using another asynchronous machine to drive the shaft of the generator. It is recommended that a turbine driven by airflow is used to drive the generator shaft in future as this is the intended application.

If the system is desired to be used as a stand-alone system, it will require a separate battery to power all the control and gate-drive circuitry.

Although the prototype circuit was able to charge the batteries, a battery management system should be considered to allow the state of charge of the various converter batteries to remain the same. Different charging algorithms should be investigated in order to find the optimal battery charging solution. As an alternative to using lead-acid batteries, the use of lithium-ion batteries as well as supercapacitors could be investigated.

A different IGBT module should be considered for the inverter circuit. The chosen module has a very high junction-to-case and case-to-sink thermal resistance. The resulting IGBT operating junction-to-ambient temperature is very high and the inverter circuit will not be able to function in areas with an ambient temperature above 40°C to 45°C.

The prototype circuit was designed as a concept demonstrator for a circuit used on board an aircraft to supply power to an electrical load. The circuit can however also be used to supply power to small loads in remote areas by replacing the RAM air turbine with a wind turbine. This could serve as a renewable energy solution in areas without access to the local power grid.

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Appendices

Appendix A

Complete Circuit Schematics

A.1 DC-DC Converter Circuit Schematics

All of the circuit diagrams used for the implementation of the bidirectional current-controller voltage-regulated dc-dc converter prototype circuit are given in this section.

A.1.1 Power Stage Schematics

The schematics for the power stage of the dc-dc converter are given in this section. It includes the half-bridge converter topologies, gate-drive circuitry and pre-charge soft-start mechanisms. The schematic for the top-half of the converter is shown in Fig. A.1 and the schematic for the bottom half is shown in Fig. A.2.

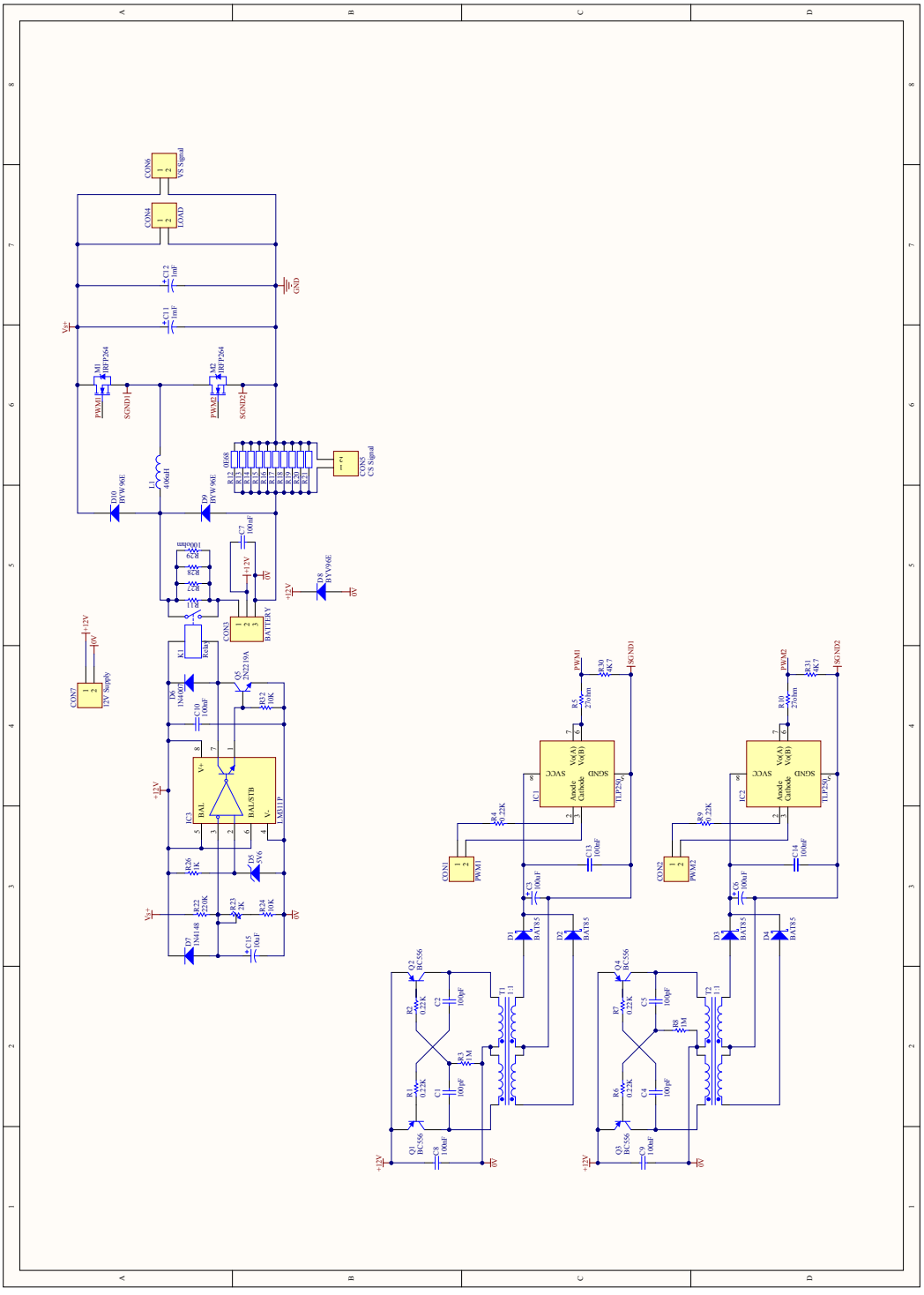

Figure A.1: Schematic for the top-half of the dc-dc converter circuit.

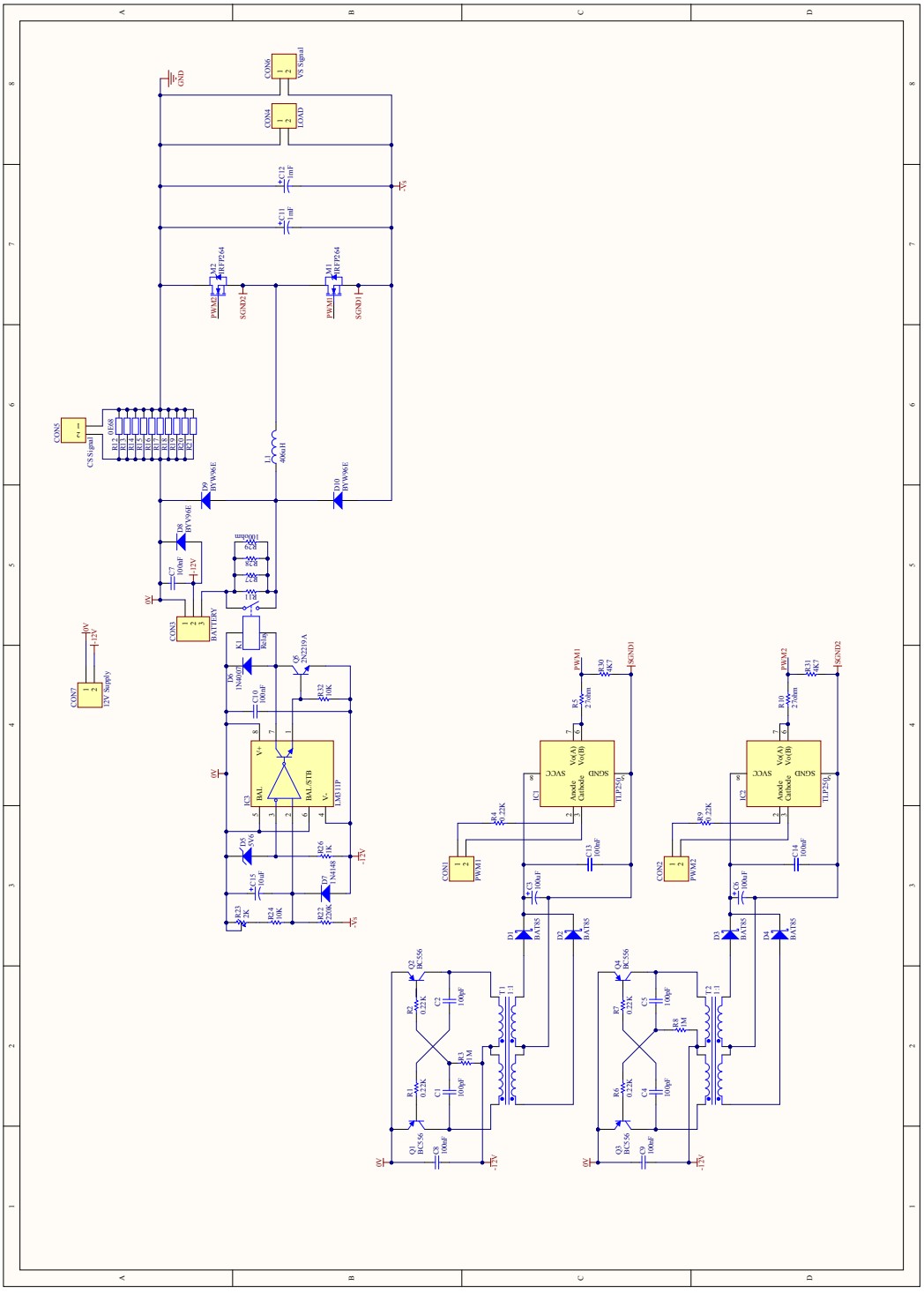

Figure A.2: Schematic for the bottom-half of the dc-dc converter circuit.

A.1.2 Control Stage Schematics

The complete control schematic for the top- and bottom-half of the dc-dc converter circuit is given in this section in Fig.A.3.

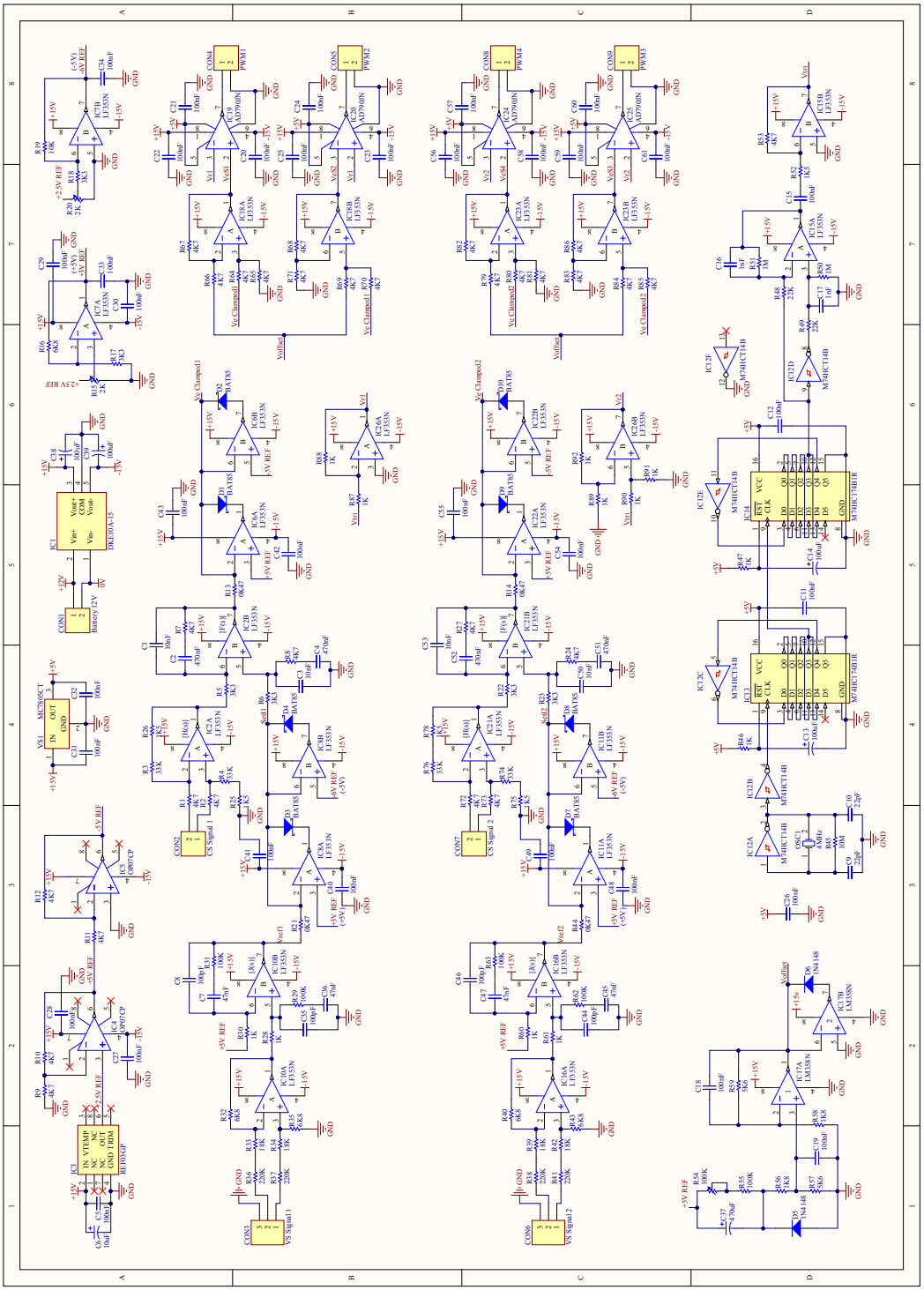

Figure A.3: Control schematic for the dc-dc converter circuit.

A.2 Inverter Circuit Schematics

All of the circuit diagrams used for the implementation of the bidirectional current-controller three-phase inverter prototype circuit are given in this section.

A.2.1 Power Stage Schematics

The schematics for the power stage of the inverter circuit are given in this section. It includes the three-phase inverter topology, gate-drive circuitry and dc bus current sensor. The schematic is shown in Fig.A.4.

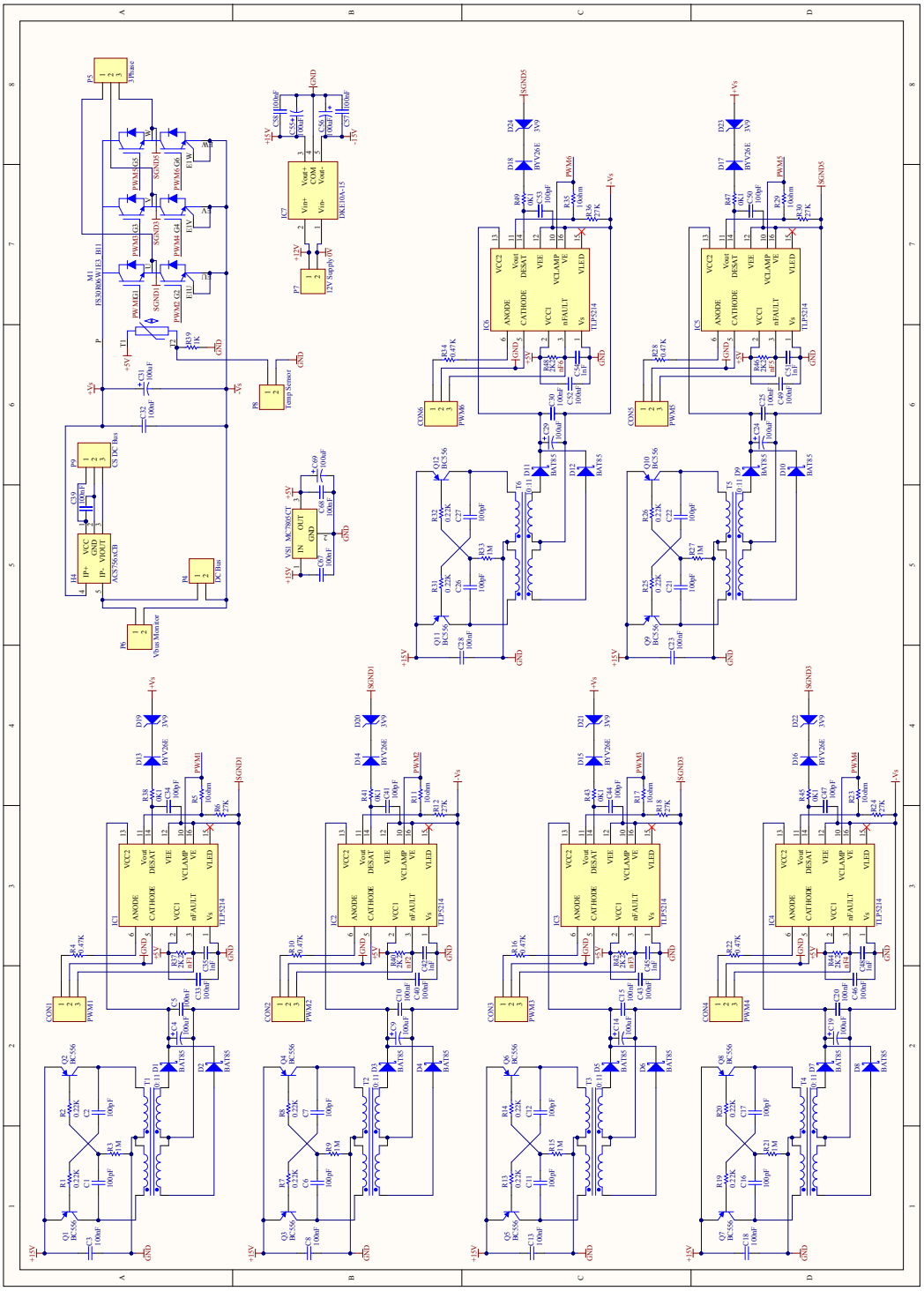

Figure A.4: Schematic for the power stage of the inverter circuit.

A.2.2 Control Stage Schematics

The complete control schematics for the three-phase inverter circuit are given in this section. The schematic containing the dsPIC, DAC and magnetic pick-up interface circuit is shown in Fig. A.5. The schematic for the analog part of the control circuit is shown in Fig. A.6.

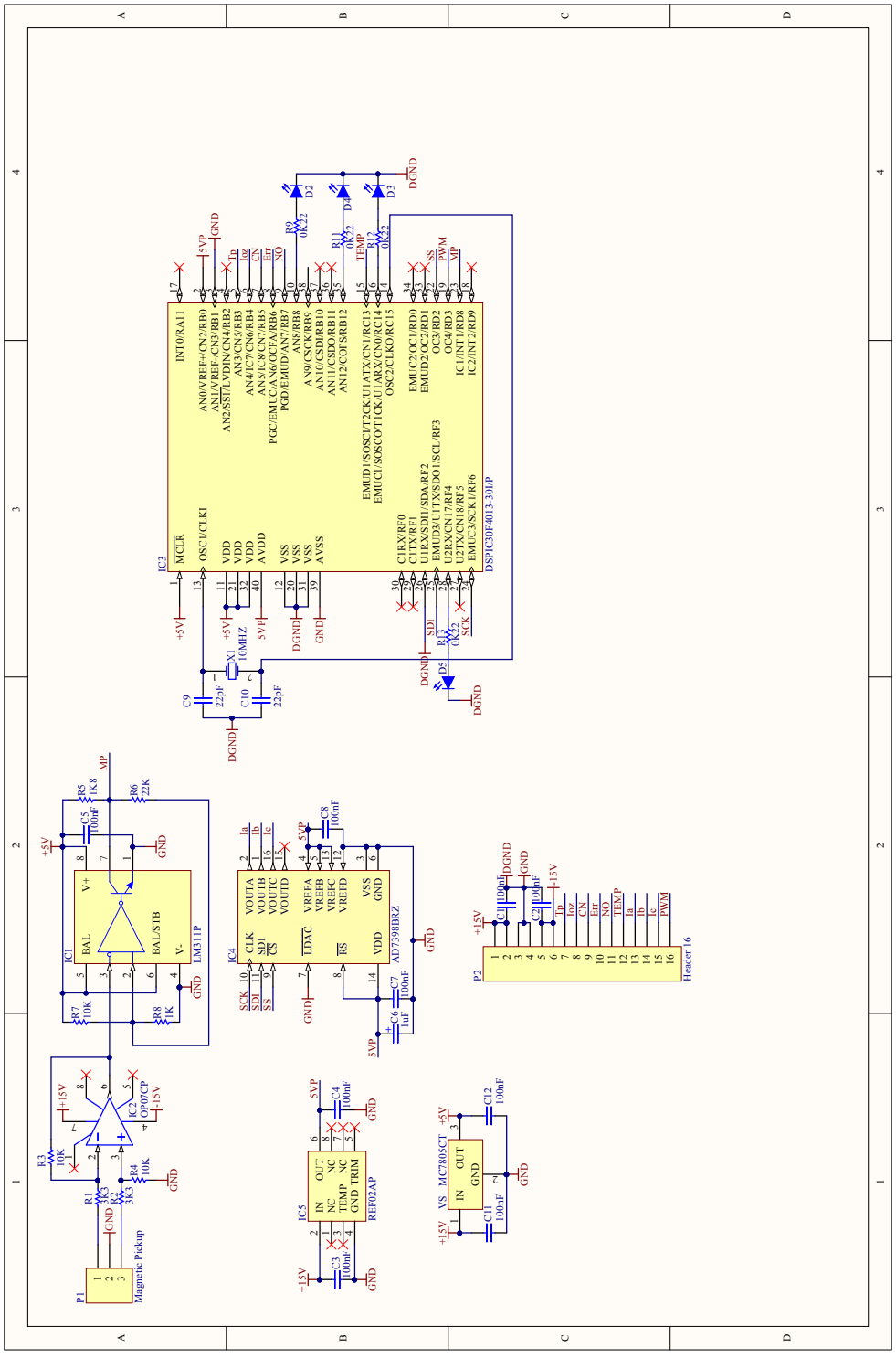

Figure A.5: Schematic for the inverter digital control circuit.

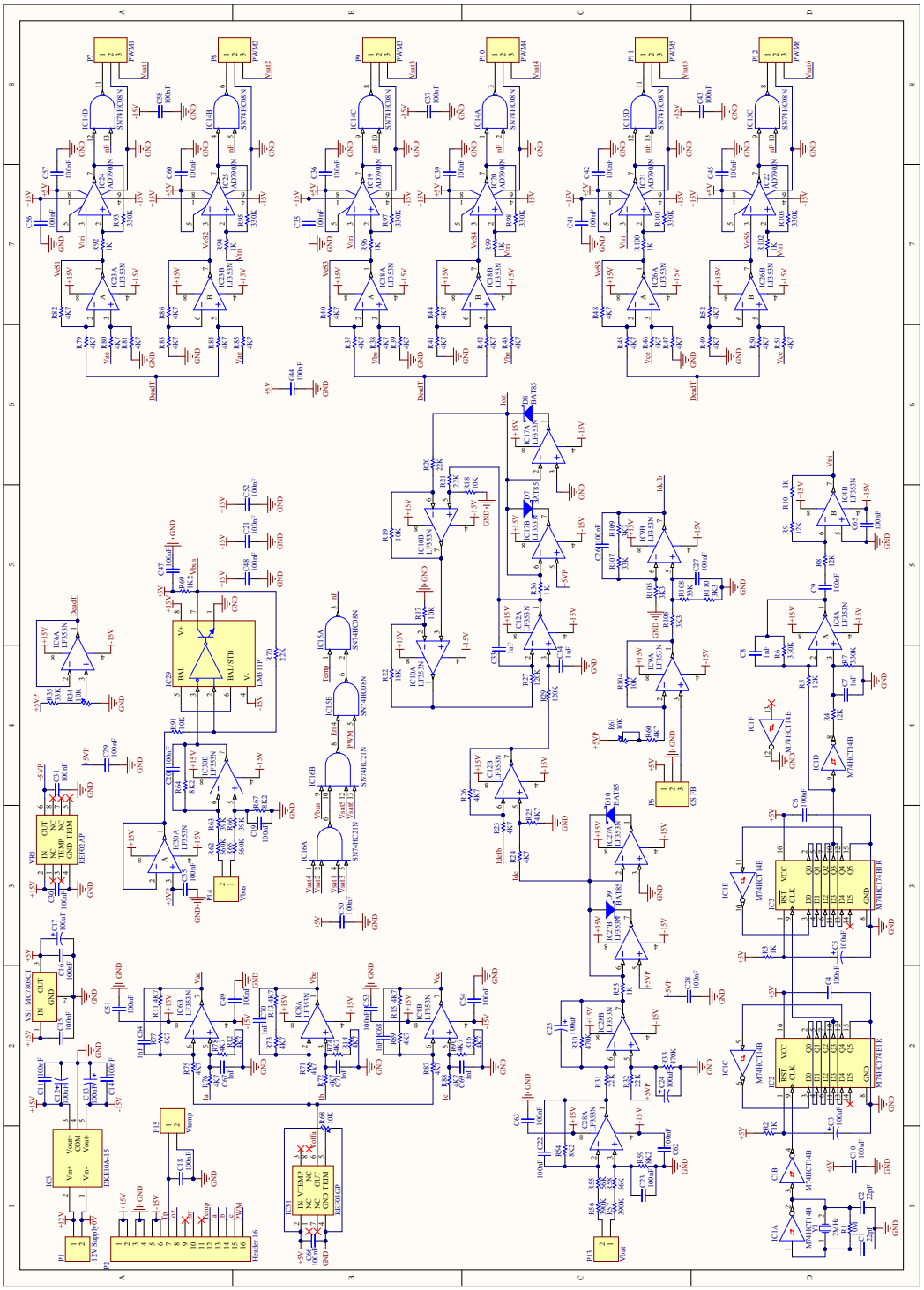

Figure A.6: Schematic for the inverter analog control circuit.

Appendix B

Printed Circuit Boards

B.1 DC-DC Converter Printer Circuit Boards

The PCBs used for the dc-dc converter prototype circuit are given in this section.

B.1.1 Power Stage PCB

The two PCBs used to generate the positive and negative dc bus are shown in Fig. B.1 and Fig. B.2 respectively. The boards are made from 70 μm copper tracks on both the top and bottom layers. Each PCB contains a half-bridge converter topology, gate-drive circuitry and a pre-charge soft-start mechanism as well as current sense resistors.

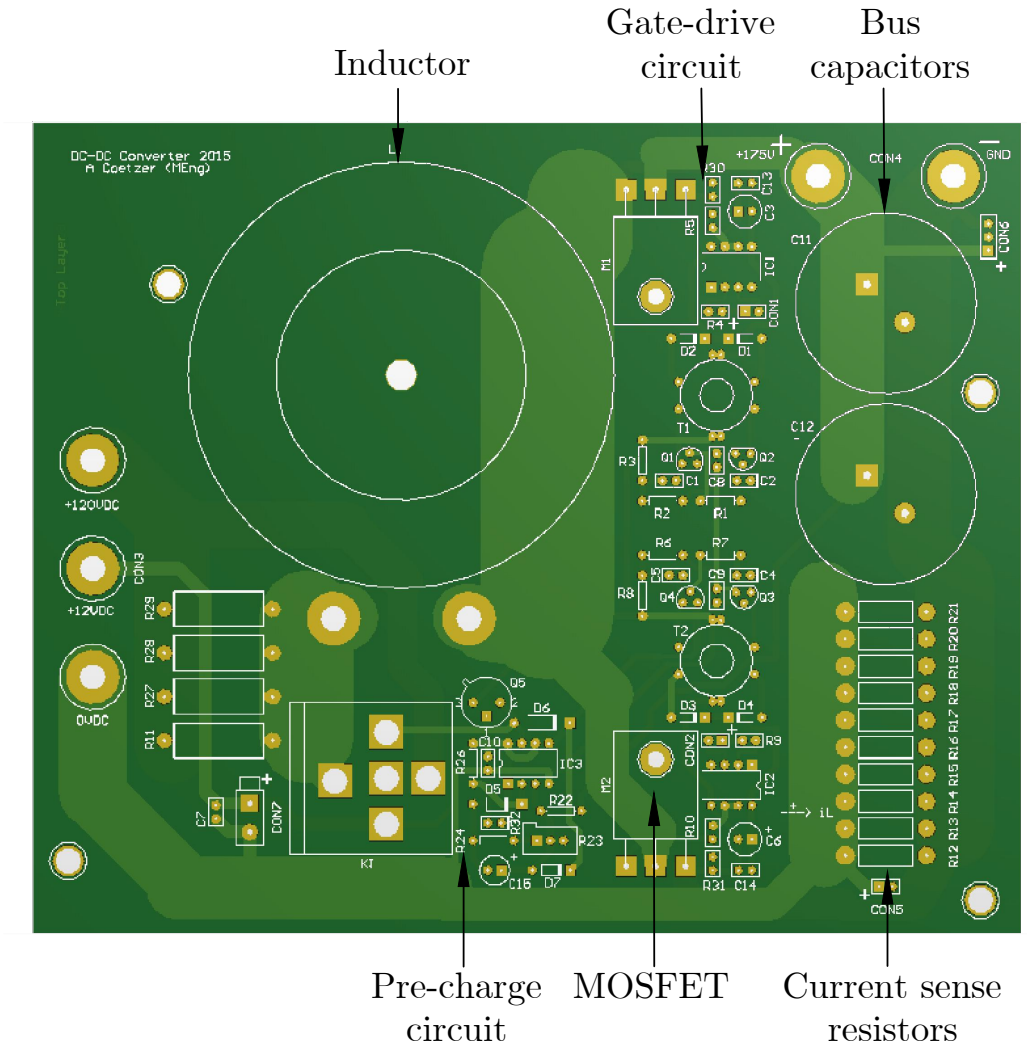

Figure B.1: PCB for the top-half of the dc-dc converter circuit producing +175 V.

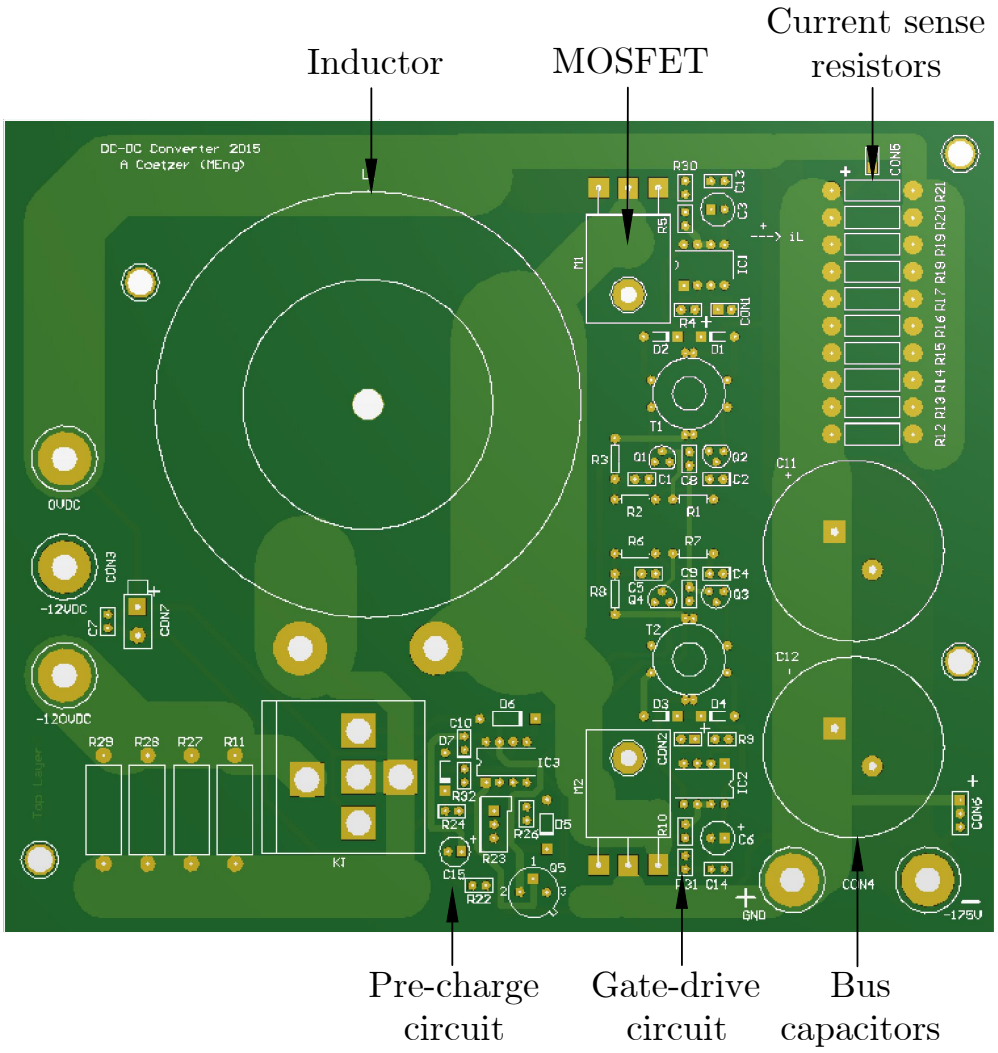

Figure B.2: PCB for the bottom-half of the dc-dc converter circuit producing -175 V.

B.1.2 Controller PCB

The two-layer PCB containing the dc-dc converter control circuit is shown in Fig. B.3. The tracks on both the top and bottom layers are made from 35 μm of copper. The PCB includes a DKE10-15A 10 W dc-dc regulated dual output (+15 V and -15 V) converter to power the control circuit from one of the 12 V batteries.

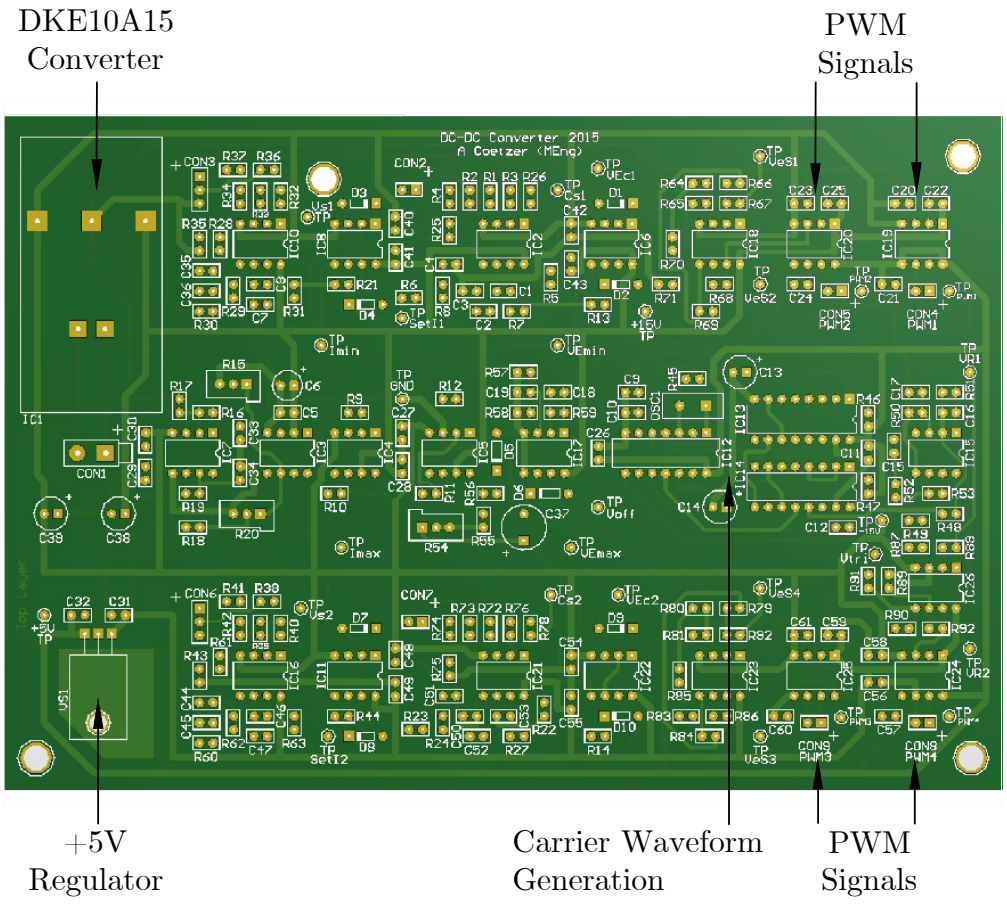

Figure B.3: Control PCB of the dc-dc converter.

B.2 Inverter Printer Circuit Boards

The PCBs used for the inverter prototype circuit are given in this section.

B.2.1 Power Stage PCB

The PCB used to implement the power stage of the inverter circuit is shown in Fig. B.4. The board is made from 70 μm copper tracks on both the top and bottom layers. The PCB contains the three-phase half-bridge inverter topology located inside the IGBT module, gate-drive circuitry and the dc bus current sensor. The PCB includes a DKE10-15A 10 W dc-dc regulated dual output (+15 V and -15 V) converter to power the gate-drive circuitry from a 12 V bench supply.

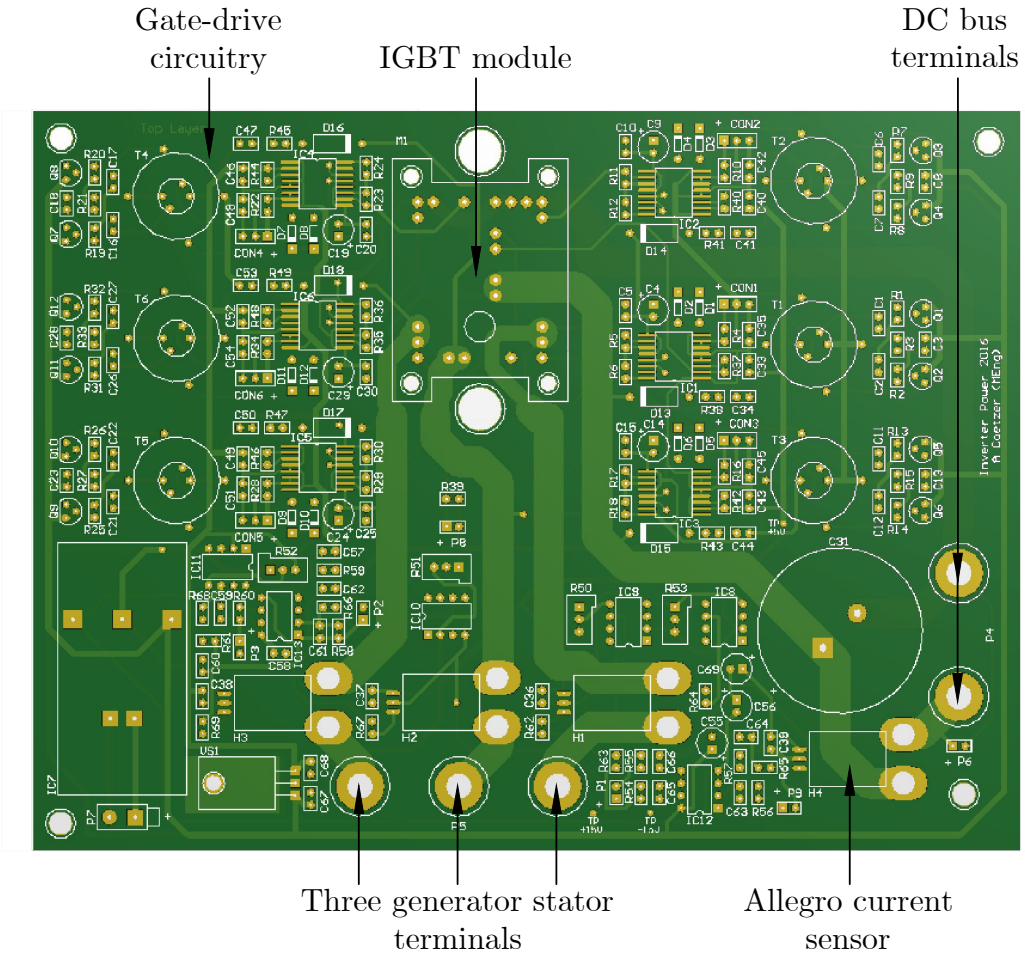

Figure B.4: PCB for the power stage of the inverter circuit.

B.2.2 Controller PCB

The two PCBs containing the control circuitry used to control the IGBTs on the power board are shown in Fig. B.5 and Fig. B.6 and contain the digital and analog control circuits, respectively. Both PCBs are two-layer boards and the tracks on the top and bottom layers are made from 35 μm of copper. The analog PCB includes a DKE10-15A 10 W dc-dc regulated dual output (+15 V and -15 V) converter to power the control circuitry on both the analog and digital PCBs from a 12 V bench power supply.

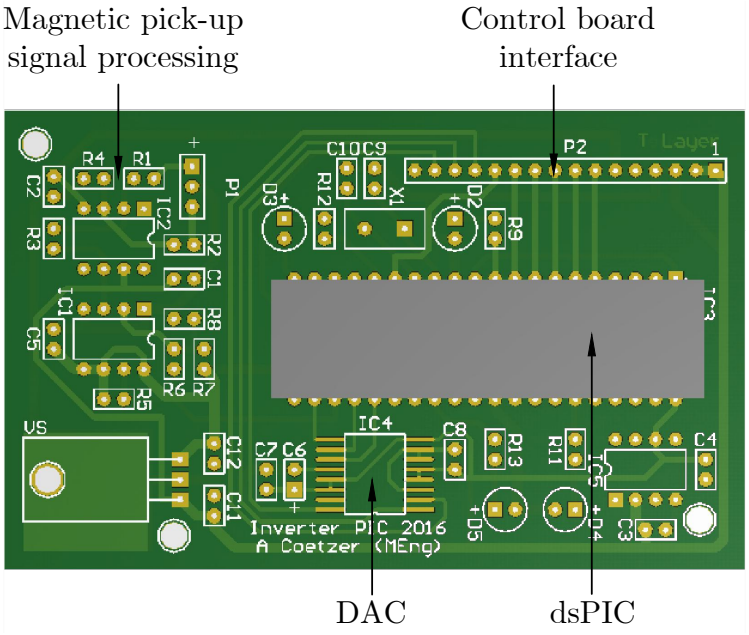

Figure B.5: PCB for the digital inverter control circuit.

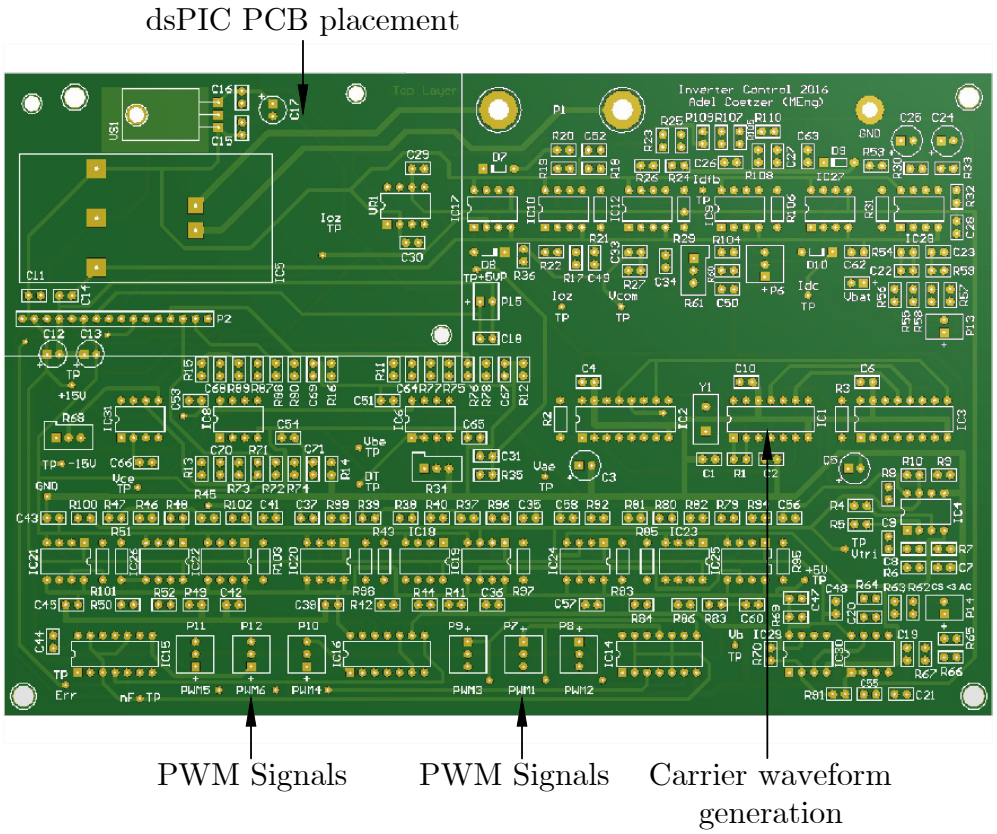

Figure B.6: PCB for the analog inverter control circuit.